TEAC FD-55E, FD-55F
MINI FLEXIBLE DISK DRIVE
SPECIFICATION

Note: This is a provisional specification and might be changed without notice.

Nov. 1981

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1-1. APPLICATION

This SPECIFICATION provides a description for the TEAC FD-55E, single sided 96tpi and the FD-55F, double sided 96tpi mini flexible disk drives (hereinafter referred to as FDD).

1-2. DISK

5.25 inch, soft or hard sectored flexible disk which is mutually agreed between TEAC and the customer.

1-3. PHYSICAL SPECIFICATION

(1) Width: 146mm (5.75 in)

(2) Height: 41.3mm (1.63 in)

(3) Depth: 203mm (7.99 in)

(4) Weight: 1.5Kg (3.31 lbs) or less

(5) External view: See Fig. 101

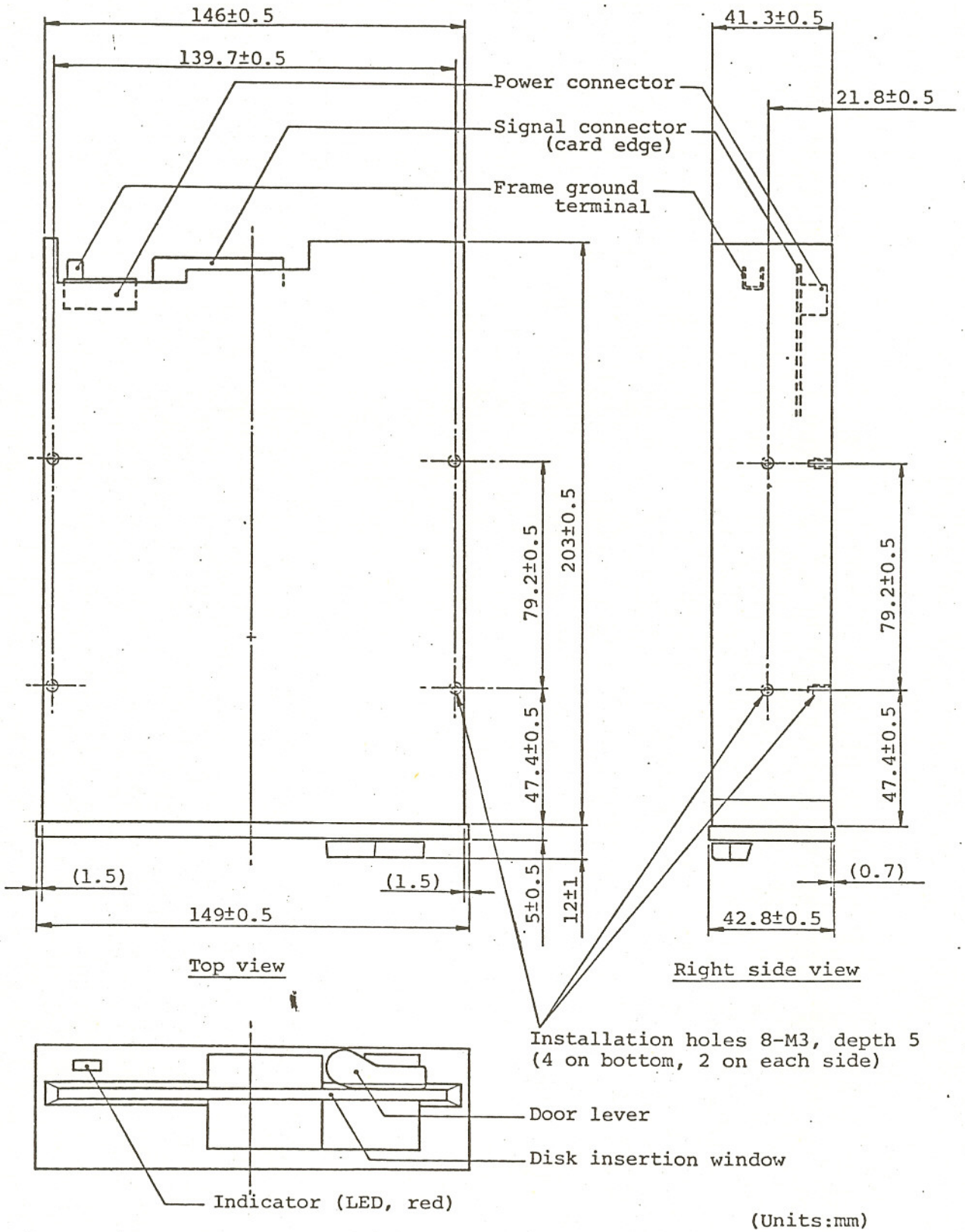
(6) Cooling: Natural air cooling

(7) Mounting: Mounting for the following three directions are acceptable.

(a) Top loading
(b) Front loading, mounted vertically with indicator up or down.
(c) Front loading, mounted horizontally with indicator up. Do not mount horizontally with spindle motor up.

(8) Installation: With the installation holes on the side panel or on the bottom panel of the FDD (see Fig.101).

(9) Material of the frame: Aluminum



(Fig.101) External view

1-4. REQUIRED POWER

The following specifications are applicable at the power connector of the FDD.

(1) DC+12V

(a) Tolerance: ±5%
(b) Allowable ripple voltage: Less than 200mVp-p (including noise)
(c) Operating current consumption
Typical: 0.3A
Maximum: 0.7A
Peak: 1.2A (400msec, Max. at spindle motor start)
(d) Waiting current consumption (spindle motor and head load solenoid are off)
Typical: 0.05A
Maximum: 0.1A

(2) DC+5V

(a) Tolerance: ±5%
(b) Allowable ripple voltage: Less than 100mVp-p (including noise)
(c) Operating current consumption
Typical: 0.55A
Maximum: 0.7A
(d) Waiting current consumption
Typical: 0.35A
Maximum: 0.45A

(3) Power consumption

(a) Typical at operating: 6.35W
(b) Typical at waiting: 2.35W

(4) Power on sequence

Not specified. Since the FDD is equipped with power reset circuit, disk and data on the disk will not be damaged by power on or off.

1-5. ENVIRONMENTAL CONDITIONS

(1) Ambient temperature

(a) Operating: 4°C ∿ 46°C (40°F ∿ 115°F)
(b) Shipping: -40°C ∿ 62°C (-40°F ∿ 144°F)
(c) Storage: -22°C ∿ 47°C (-8°F ∿ 117°F)

(2) Relative humidity

(a) Operating: 20% ∿ 80% (no condensation, Maximum wet bulb temp.:29°C,84°F)
(b) Shipping: 1% ∿ 95% (no condensation)
(c) Storage: 1% ∿ 95% (no condensation)

(3) Vibration, operating: Less than 0.25G (less than 50Hz)

1-6. OPERATIONAL CHARACTERISTICS

(1) Read/Write performance

Models			FD-55E (Single sided)	FD-55F (Double sided)
Recording method			MF or MFM	MF or MFM
Data transfer rate (K bits/sec)			250	250
Tracks/disk			160	160
Innermost track bit density (bpi)			5576	5592(side 1)
Data capacity	Unformatted	K bytes/track	6.25	6.25
		K bytes/disk	500	1000
	Formatted (16 sectors /track)	K bytes/sector	0.256	0.256
		K bytes/track	4.096	4.096
		K bytes/disk	327.68	655.36

Note: The numerical values in the table show the case of MFM recording method.

(Table 101) Read/write performance

(2) Disk rotation mechanism

(a) Spindle motor: Direct DC brushless motor

(b) Spindle motor speed: 300rpm

(c) Motor servo method: Frequency servo by AC tachometer

(d) Motor/spindle connection: Motor shaft direct

(e) Disk speed: 300rpm

Long term speed variation (LSV): Less than $\pm$1.5%

Instantaneous speed variation (ISV): Less than $\pm$2.0%

(f) Start time: Less than 400msec

(g) Average latency: 100msec

(3) Index

(a) Number of index: 1/revolution

(b) Detection method: LED and photo-transistor

(c) Detection cycle: 200msec ± 1.5%

(d) Index/alignment dipole spacing: 0 ∿ 400μsec, with specified test disk

(4) Track construction

(a) Track density: 96tpi

(b) Number of tracks

FD-55E: 80 tracks

FD-55F: 80 tracks/surface, 160 tracks/disk

(c) Outermost track radius (track 00)

FD-55E: 57.150mm (2.2500 in)

FD-55F: Side 0 57.150mm (2.2500 in)

Side 1 55.033mm (2.1667 in)

(d) Innermost track radius (track 79)

FD-55E: 36.248mm (1.4271 in)

FD-55F: Side 0 36.248mm (1.4271 in)

Side 1 34.131 (1.3438 in)

(5) Magnetic head

(a) Magnetic head: Read/write head with tunnel erase

(b) Read/write track width: 0.159mm

(c) Erase track width: 0.097mm

(d) Read write/erase gap spacing: 0.85 ± 0.05mm

(6) Track seek mechanism

(a) Head positioning mechanism: Band positioner

(b) Step motor: 4-phase, 1.8°/1 step, 1 step/1 track

(c) Track 00 and innermost stopper
Mechanical moving stopper of head carriage

(d) Track 00 detection method: LED and photo-transistor

(e) Track to track time: Less than 3msec

(f) Settling time: Less than 15msec

(g) Average track access time: 94msec

(7) Head load mechanism

(a) Head load mechanism: Solenoid

(b) Head load time: Less than 50msec

(c) Option: Contact start/stop type (without solenoid)

(8) File protect mechanism: Detection of write enable notch by LED and photo transistor

1-7. RELIABILITY

(1) MTBF: 8,000 power on hours

(2) MTTR: 30 minutes

(3) Component life: 5 years

(4) Preventive maintenance: Not required

(5) Media life: 3.0×10^6 passes per track

(6) Error rates

(a) Soft read error: 1 per 10^9 bits (up to 2 retries)
(b) Hard read error: 1 per 10^{12} bits
(c) Seek error: 1 per 10^6 seeks

(7) Security standard: Complying with UL

1-8. SIGNAL INTERFACE

Four FDDs, Max. can be connected to one FDD control unit by daisy chaining.

1-8-1. Circuit and Electrical Characteristics

(1) Interface driver/receiver: See Fig.102.

(2) Electrical characteristics

The following specifications are applicable at the signal connector of the FDD.

(a) Input signal

LOW level (TRUE): 0V ∿ 0.5V

Terminator current: -36mA, Max.

FDD PCBA current: -2.5mA, Max.

HIGH level (FALSE): 2.5V ∿ 5.25V

(b) Output signal

LOW level (TRUE): 0V ∿ 0.4V

Sink current capability: 48mA, Max.

HIGH level (FALSE): 5.25V, Max. (open collector)

(3) Terminator

(a) Resistance: 150Ω ± 5%

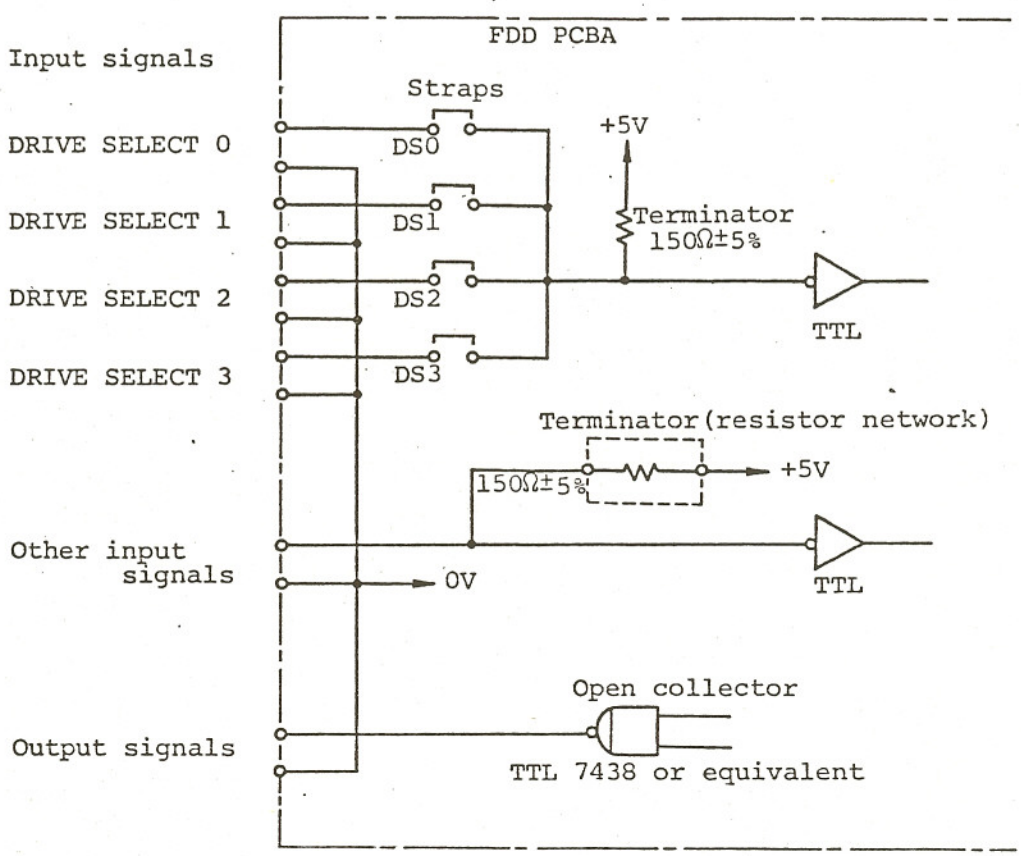
(b) Terminator for DRIVE SELECT 0 ∿ 3 input signals:
A terminator resistor is mounted on the PCB with soldering joint.

(c) Terminator for other input signals:
A resistor network is mounted on IC socket on the PCB.

(d) Shipping condition:
All of the terminator resistors are mounted.

(e) Multiplex connection:

For the multiplex connection of the FDDs by daisy chaining, the resistor network explained in item (c) shall be removed from all the FDDs except for the final FDD of the interface cable.



(Fig.102) Interface driver/receiver

1-8-2. Signal Connector and Cable

(1) Signal connector

(a) FDD side connector: Card edge (gold plated)

(b) Pin numbers & pin pitch: 34 pins, 2.54mm (0.1 in) pitch
(17 pins on both sides, even number pins are bottom side of the FDD)

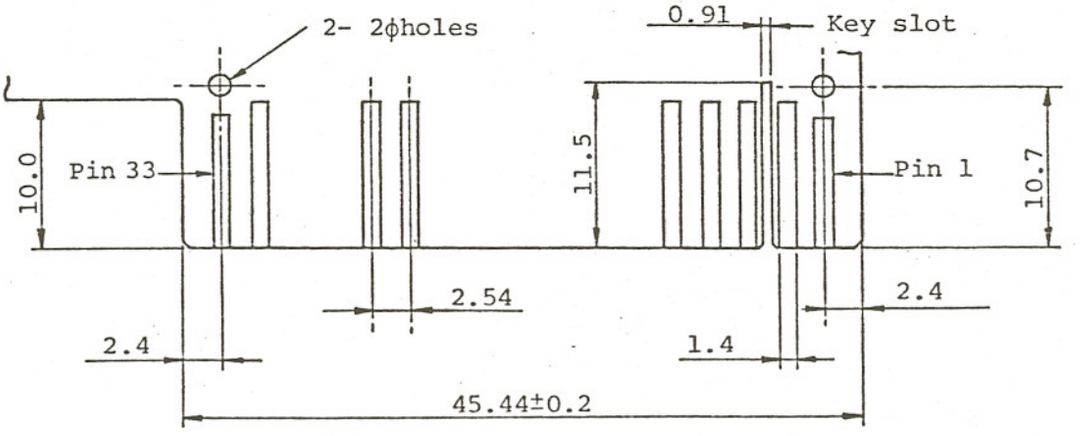
(c) Polarizing key location: Between pins 4 and 6

(d) Card edge dimensions: See Fig.103

(e) Interface connections: See Table 102

(f) Cable side matched connector: 3M, Scotchflex ribbon connector, P/N 3463-0001
or AMP, thin leaf connector, P/N 583717-5
and contactor P/N 1-583616-1
or equivalent

(2) Maximum interface cable length: 3m, Max.
For the multiplex connection by daisy chaining, the total cable length shall be less than 3m.



PCB thickness: 1.6, nominal
(Units: mm)

(Fig.103) Card edge dimensions of signal connector

Signals	Directions	Terminal Nos.	
		Signals	0V
RESERVED	INPUT	2	1
IN USE	INPUT	4	3
DRIVE SELECT 3	INPUT	6	5
INDEX/SECTOR	OUTPUT	8	7
DRIVE SELECT 0	INPUT	10	9
DRIVE SELECT 1	INPUT	12	11
DRIVE SELECT 2	INPUT	14	13
MOTOR ON	INPUT	16	15
DIRECTION SELECT	INPUT	18	17
STEP	INPUT	20	19
WRITE DATA	INPUT	22	21
WRITE GATE	INPUT	24	23
TRACK 00	OUTPUT	26	25
WRITE PROTECT	OUTPUT	28	27
READ DATA	OUTPUT	30	29
SIDE ONE SELECT	INPUT	32	31
READY	OUTPUT	34	33

Note: SIDE ONE SELECT signal is used only for the FD-55F.

(Table 102) Signal interface connections

1-8-3. Input/Output Signals

In the following, input signals are those transmitted to the FDD while output signals are those transmitted from the FDD.
LOW level of the signals is TRUE.

(1) DRIVE SELECT 0 ∿ 3 input signals

(a) Level signals of four lines to select a specific FDD for operating in multiplex control by daisy chaining.
(b) When the MX strap is on, only the DRIVE SELECT signal of the same number as of on-state strap among DS0 ∿ 3 straps is effective.
(c) All the output signals and all the input signals except for the MOTOR ON and the IN USE signals can be effective when this signal is effectively received or when the MX strap is off.
(d) The time required to make each input or output signal effective after the transmission of this signal is 0.5μsec, Max. including delay time through the interface cable.
(e) When the DRIVE SELECT signal of the same number as of on-state strap among DS0 ∿ 3 straps becomes TRUE (independent of the MX strap), the indicator on the front panel turns on.
If the HS strap is on at this time and the READY signal is TRUE, head loading will be started.
Head loading will be completed within 50msec after this signal becomes TRUE.

(2) MOTOR ON input signal

(a) Level signal to rotate the spindle motor.
(b) The spindle motor reaches to the rated rotational speed within 400msec after this signal becomes TRUE.
(c) When the HM strap is on, head loading will be started after the READY signal becomes TRUE.
Head loading will be completed within 50msec after the READY signal

becomes TRUE.

(3) DIRECTION SELECT input signal

(a) Level signal to define the moving direction of the head when the STEP line is pulsed.
(b) Step-out (moving away from the center of the disk) is defined as HIGH level of this signal. Conversely, step-in (moving toward the center of the disk) is defined as LOW level of this signal.

(4) STEP input signal

(a) Pulse signal to move the head. The pulse width shall be more than 0.8μsec and the head moves one track space per one pulse.
(b) The access motion is initiated at the trailing edge of the pulse and completes within 18msec after starting the access including the settling time. For the successive access motion in the same direction, the pulses shall be input with the space of more than 3msec, while the pulses shall be input with the space of more than 18msec for the access motion in a different direction.
(c) This signal becomes ineffective when the WRITE PROTECT signal is FALSE and the WRITE GATE signal is TRUE.
(d) This signal shall be input according to the timing in Fig.104.

(5) WRITE GATE input signal

(a) Level signal to erase the written data and to enable the writing of new data.
(b) This signal becomes ineffective when the WRITE PROTECT signal is TRUE or when the READY signal is FALSE.
(c) This signal shall be made TRUE after satisfying all of the following four conditions.
    i) The FDD is in ready state (refer to item (12)).
    ii) More than 50msec after the head loading is started.

iii) More than 18msec after the effective receival of the final STEP pulse.

iv) More than 100μsec after the level change of the SIDE ONE SELECT signal.

(6) WRITE DATA input signal

(a) Pulse signal to designate the contents of the data to be written on the disk. The pulse width shall be more than 0.15μsec and the leading edge of the pulse is used.

(b) This signal becomes ineffective when one of the following conditions is satisfied.

i) WRITE GATE signal is FALSE.

ii) WRITE PROTECT signal is TRUE.

iii) READY signal is FALSE.

(c) This signal shall be input according to the timing in Fig.105.

(7) SIDE ONE SELECT input signal (for FD-55F only)

(a) Level signal to define which side of a two-sided disk is used for reading or writing.

(b) When this signal is HIGH level, the magnetic head on the side 0 surface of the disk is selected, while the magnetic head on the side 1 surface is selected when this signal is LOW level.

(c) The READ DATA signal on a selected surface becomes effective more than 100 sec after the change of this signal level.

(d) Write operation (WRITE GATE signal TRUE) on a selected surface shall be started more than 100μsec after the change of this signal level.

(e) When the other side of the disk is selected after the completion of a write operation, the level of this signal shall be switched more than 1msec after making the WRITE GATE signal FALSE.

(8) TRACK 00 output signal

(a) Level signal which indicates that the head is on track 00 (the outermost track).

(b) This signal becomes effective more than 3msec after the effective receival of the STEP pulse.

(c) If a step-out command is input at track 00, the head is shifted a little outside from the track 00 position and the TRACK 00 signal becomes FALSE immediately after the input of the step command. If a step-out command or additional three step-in commands are input at the position, the head correctly returns to the track 00 position and the TRACK 00 signal becomes TRUE.

(9) INDEX/SECTOR output signal

(a) Pulse signal for the detection of the index hole or the sector holes.

(b) This signal becomes effective 400msec after the spindle motor starts rotation.

(c) When using a soft sectored disk, there will be one index pulse on this line per one revolution of the disk. When using a hard sectored disk, sector pulse and index pulse are output together.

(d) Fig.106 shows the timing for this signal. Leading edge of the pulse shall be used as the reference.

(e) If the output conditions in item (1)-(c) are satisfied when no disk is inserted, this signal maintains TRUE.

(10) READ DATA output signal

(a) Pulse signal for the read data from the disk composing clock bits and data bits together.

(b) Fig. 107 shows the timing for this signal. Leading edge of the pulse shall be used as the reference.

(c) This signal becomes valid when all of the following five conditions are satisfied.

i) The FDD is in ready state (refer to item (12)).

ii) More than 50msec after the head loading is started.

iii) More than 18msec after the effective receival of the final STEP pulse.

iv) More than 1msec after the WRITE GATE signal becomes FALSE.

v) More than 100μsec after the level change of the SIDE ONE SELECT signal.

(11) WRITE PROTECT output signal

(a) Level signal which indicates that the write enable notch of the disk is masked.

(b) When this signal is TRUE, the data on the disk are protected from erasing and the writing of new data is inhibited.

(12) READY output signal

(a) Level signal which indicates that the FDD is in ready state.

(b) The FDD becomes ready state when all of the following four conditions are satisfied.

i) The FDD is powered on.

ii) Disk is installed.

iii) The disk rotates at nominal speed.

iv) Two INDEX pulses have been counted after the disk starts rotation.

(c) Required time for this signal to become TRUE after the MOTOR ON signal becomes TRUE is less than 800msec.

(d) If a hard sectored disk is used for the FDD, the above items (b)-iii), (b)-iv), and (c) cannot be applied. In such case, the ready state must be regarded as follows.

i) The FDD is powered on.

ii) Disk is installed.

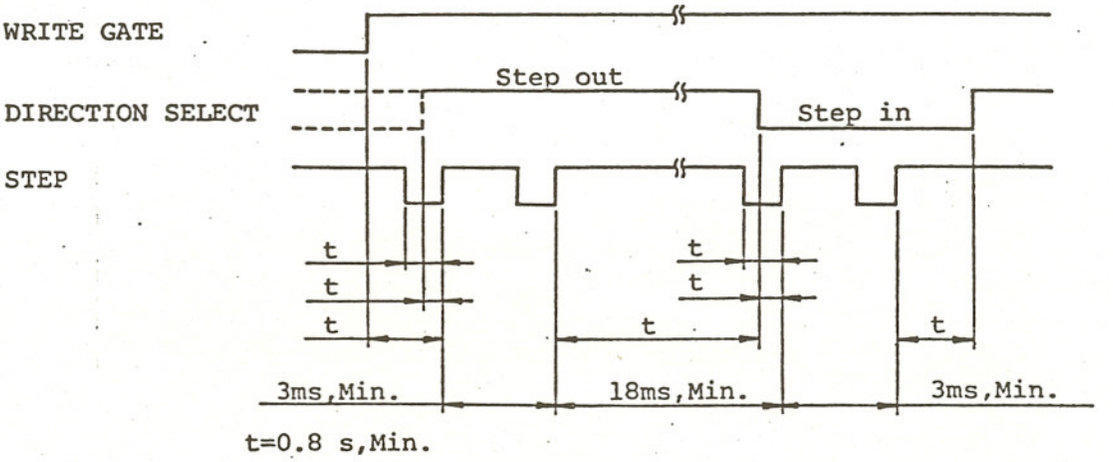
iii) More than 400msec after the MOTOR ON signal becomes TRUE.

(13) IN USE input signal

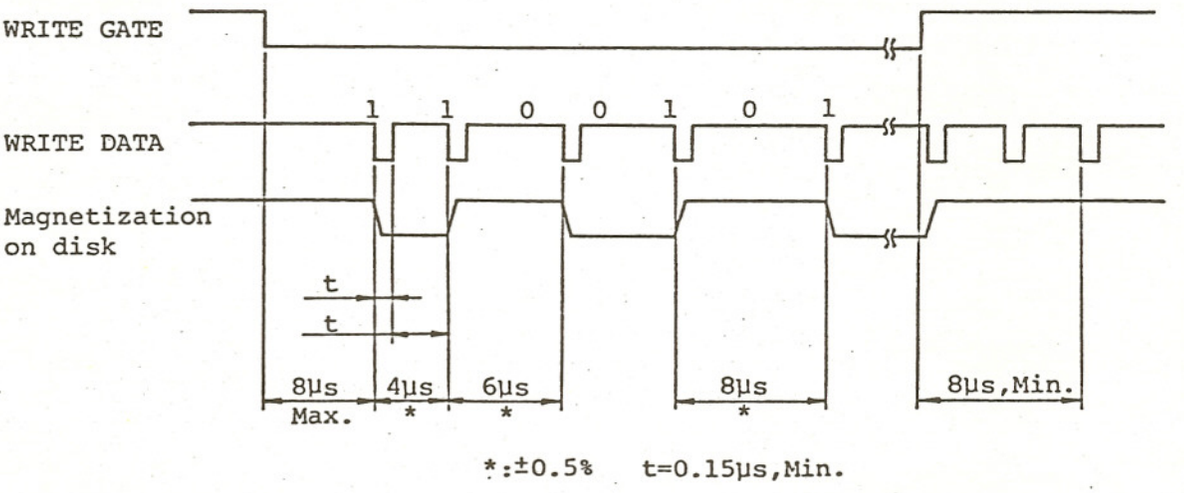
(a) Level signal to indicate that all of the daisy chained FDDs are

in use condition under the control of the host system.

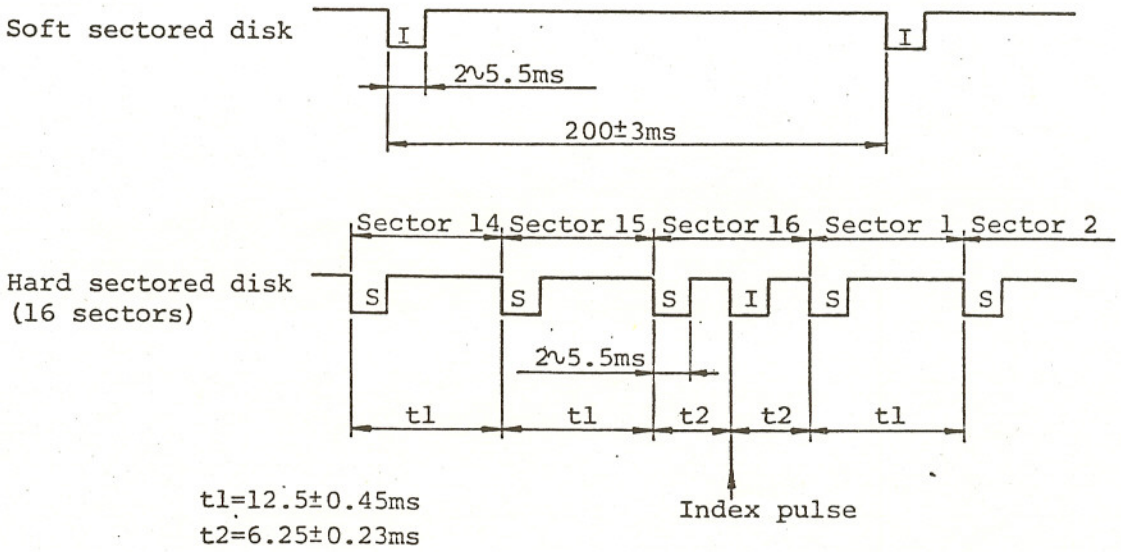
(b) The indicator on the frint panel turns on when this signal becomes TRUE.



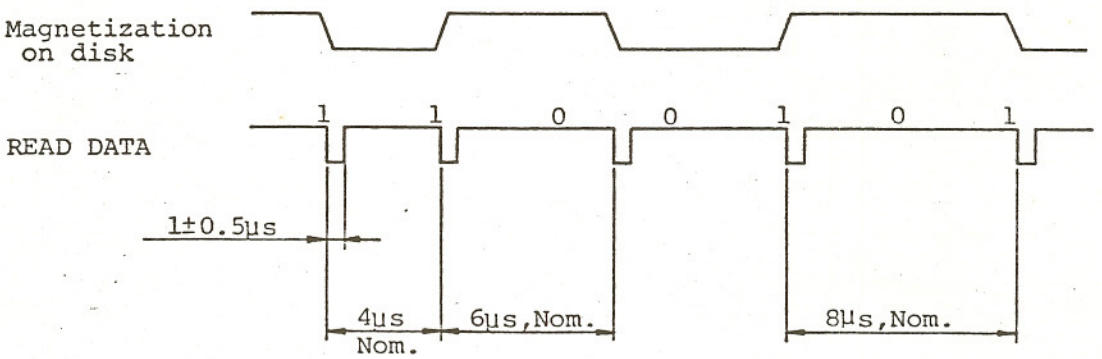
(Fig.104) STEP timing



(Fig.105) WRITE DATA timing (MFM method)



(Fig.106) INDEX/SECTOR timing



Note: The displacement of any bit position does not exceed ±20% from its nominal position.

(Fig.107) READ DATA timing (MFM method)

1-9. POWER INTERFACE

Refer to item 1-4 for power requirements.

(1) Power connector

(a) FDD side connector: AMP, Mate-N-Lock connector, P/N 350211-1 or equivalent

(b) Pin numbers: 4 pins

(c) Protection method for mis-connection: Mechanical protection by the shape of the connector housing.

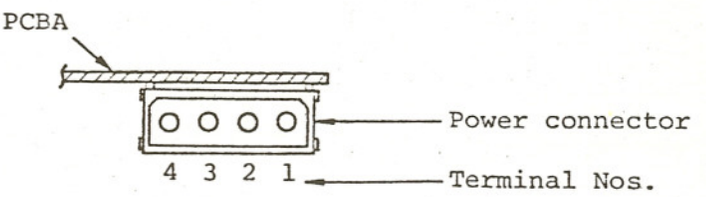
(d) Pin location: See Fig.108

(e) Power interface connections: See Table 104

(f) Cable side matched connector: AMP, P/N 1-480424-0 and pins 60617-1, or 60619-1, or equivalent

(2) Power cable

Any appropriate cables taking the maximum power consumption of the FDD and the power voltage at the connector into consideration will be acceptable.



(Fig.108) Power connector pin location (Rear view)

Voltage	Terminal Nos.
DC+12V	1
0V	2
0V	3
DC+5V	4

(Table 103) Power interface connections

1-10. FRAME GROUNDING

(1) Frame ground

(a) Frame ground is AC coupled to DC 0V by 0.01μF// 100KΩ.

(b) Insulation resistance is more than 80KΩ at less than DC 25V.

(2) Separation of the frame ground

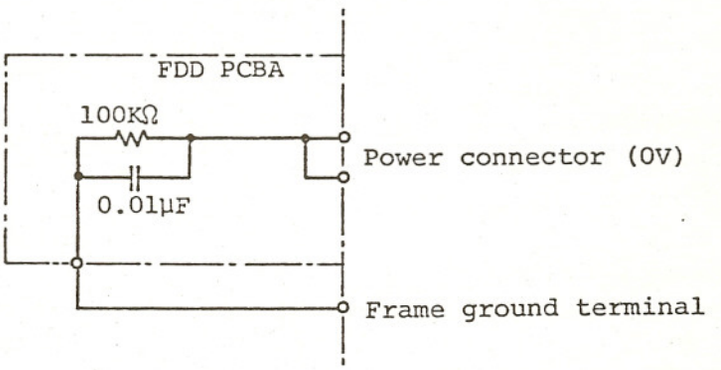
(a) Separating method: Remove 0.01μF// 100KΩ.

(b) Terminal for the separated frame ground.

Use the frame ground terminal at the back side of the FDD.

FDD side terminal: AMP faston 187 tab P/N 170001-2
or equivalent

Cable side matched terminal: AMP P/N 60972-2 or equivalent



(Fig.109) Frame ground internal connection