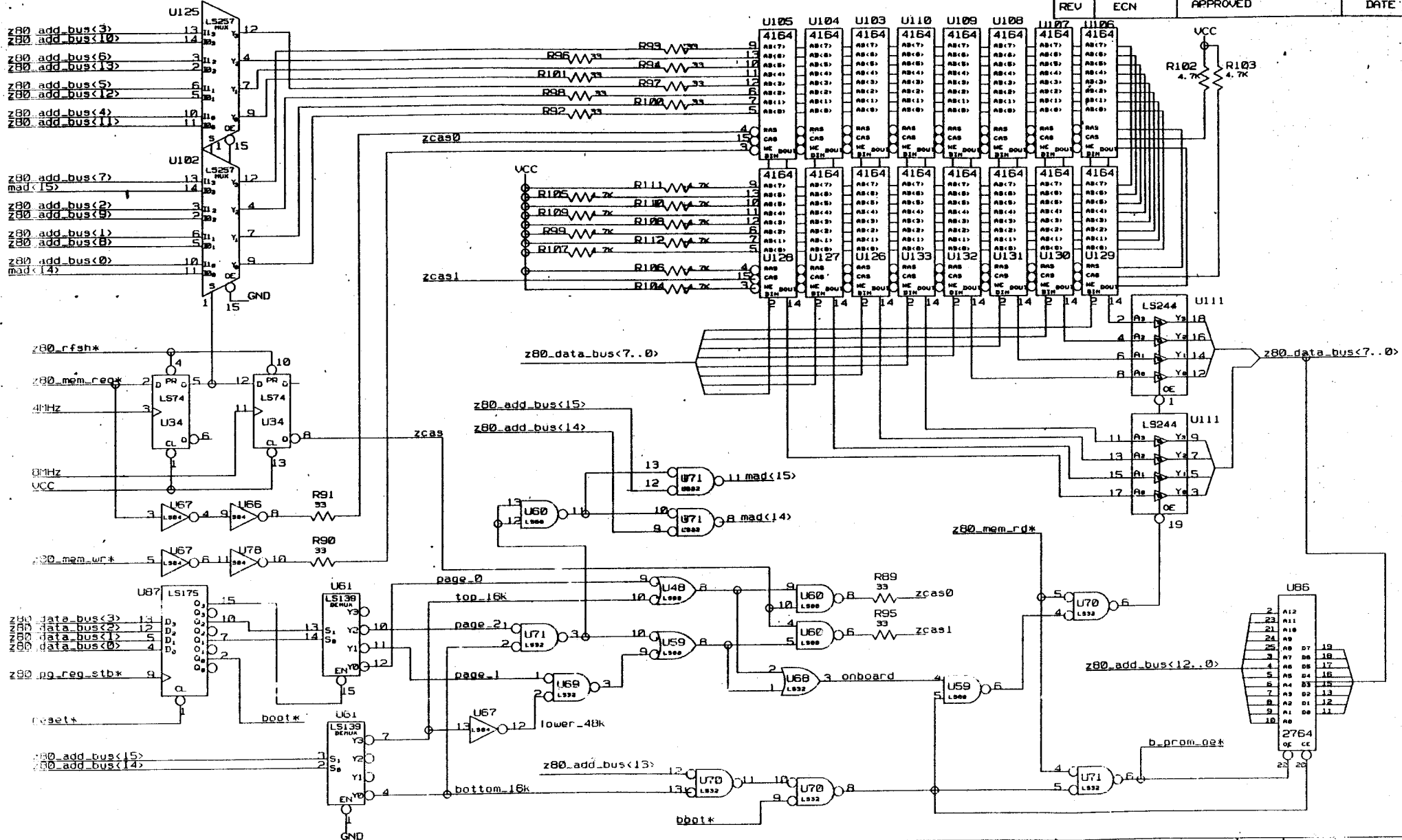


Z80 CPU and CONTROL

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REV	ECN	APPROVED	DATE
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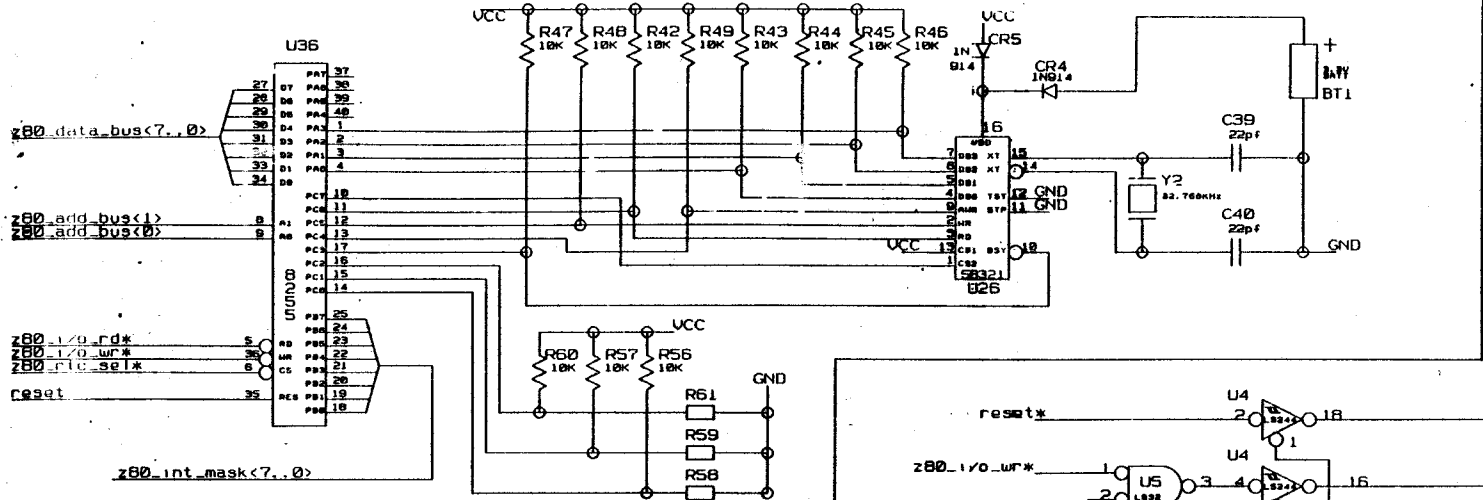
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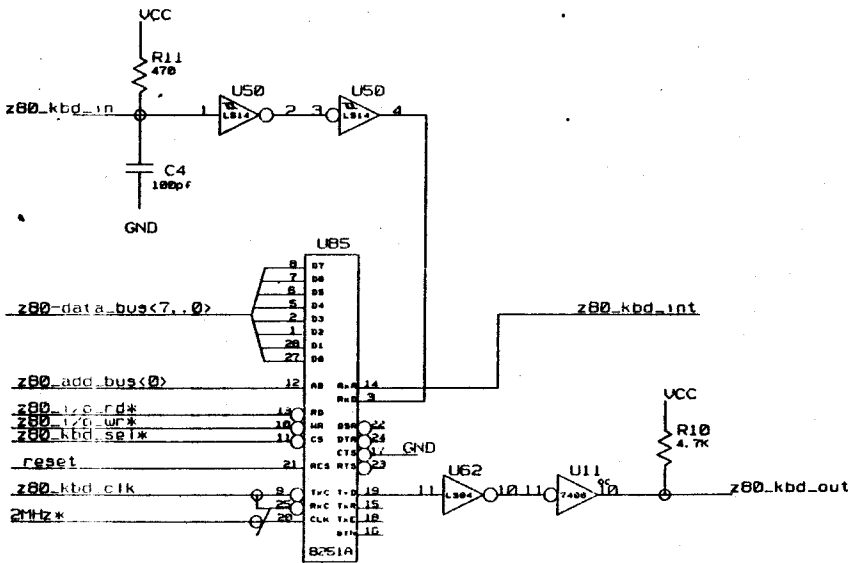
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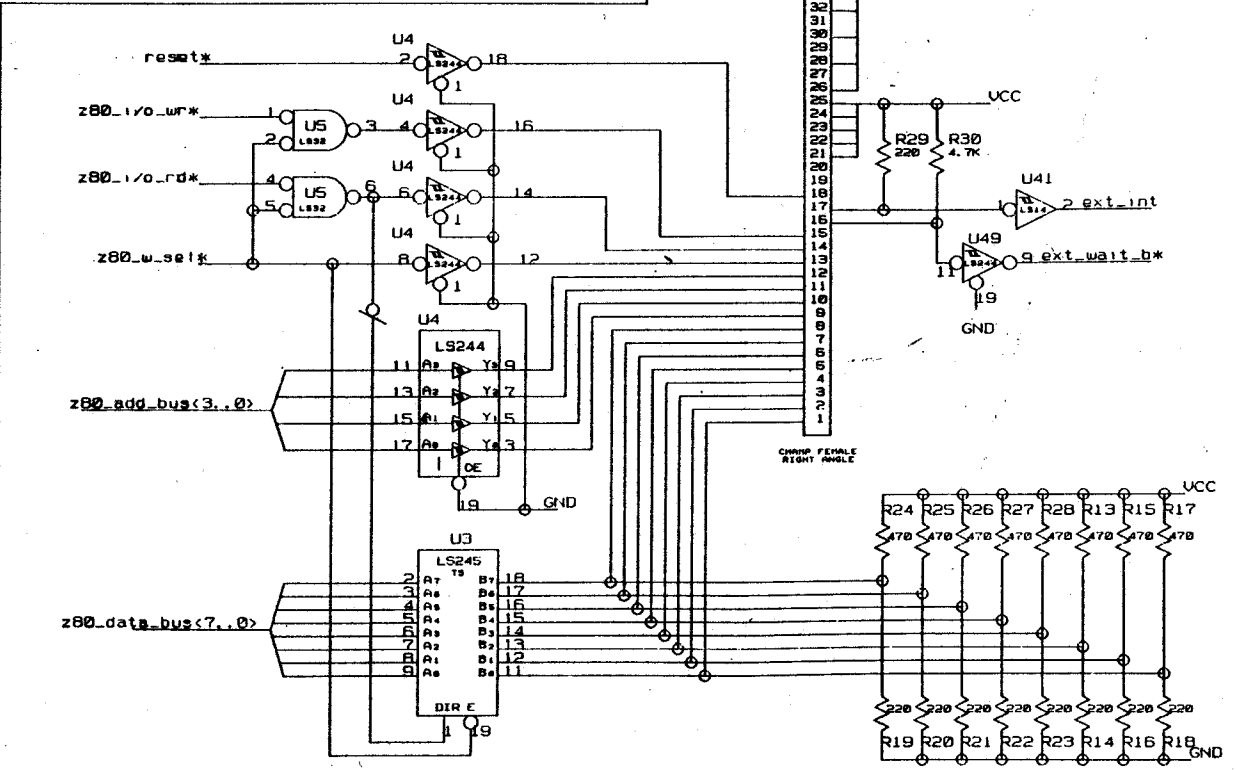
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REAL TIME CLOCK & INTERRUPT MASK



KEYBOARD INTERFACE



WINCHESTER INTERFACE

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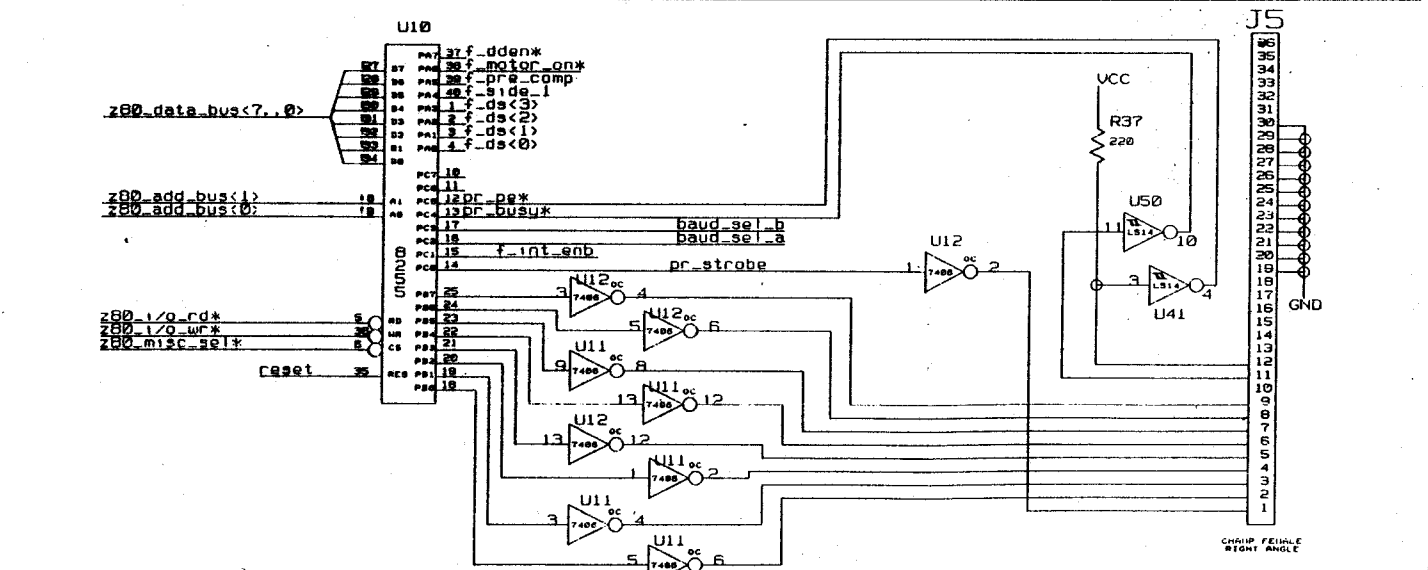
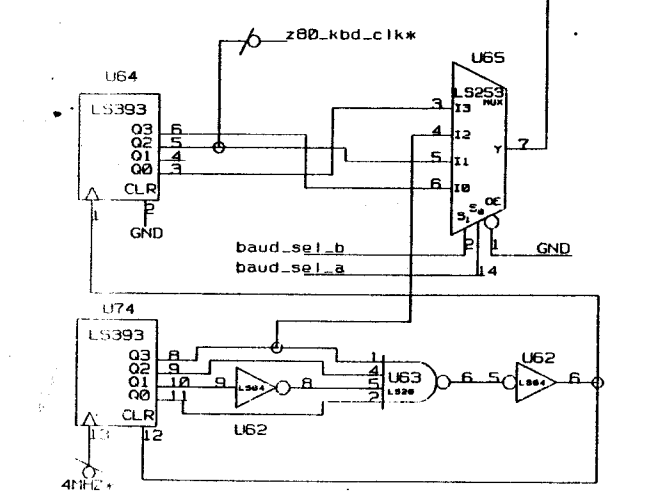
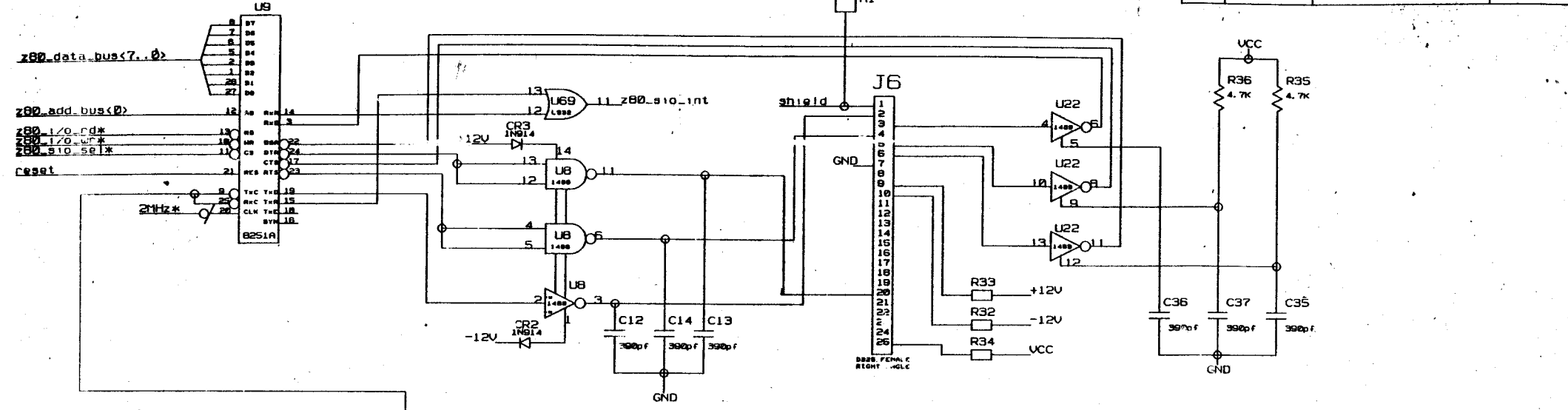
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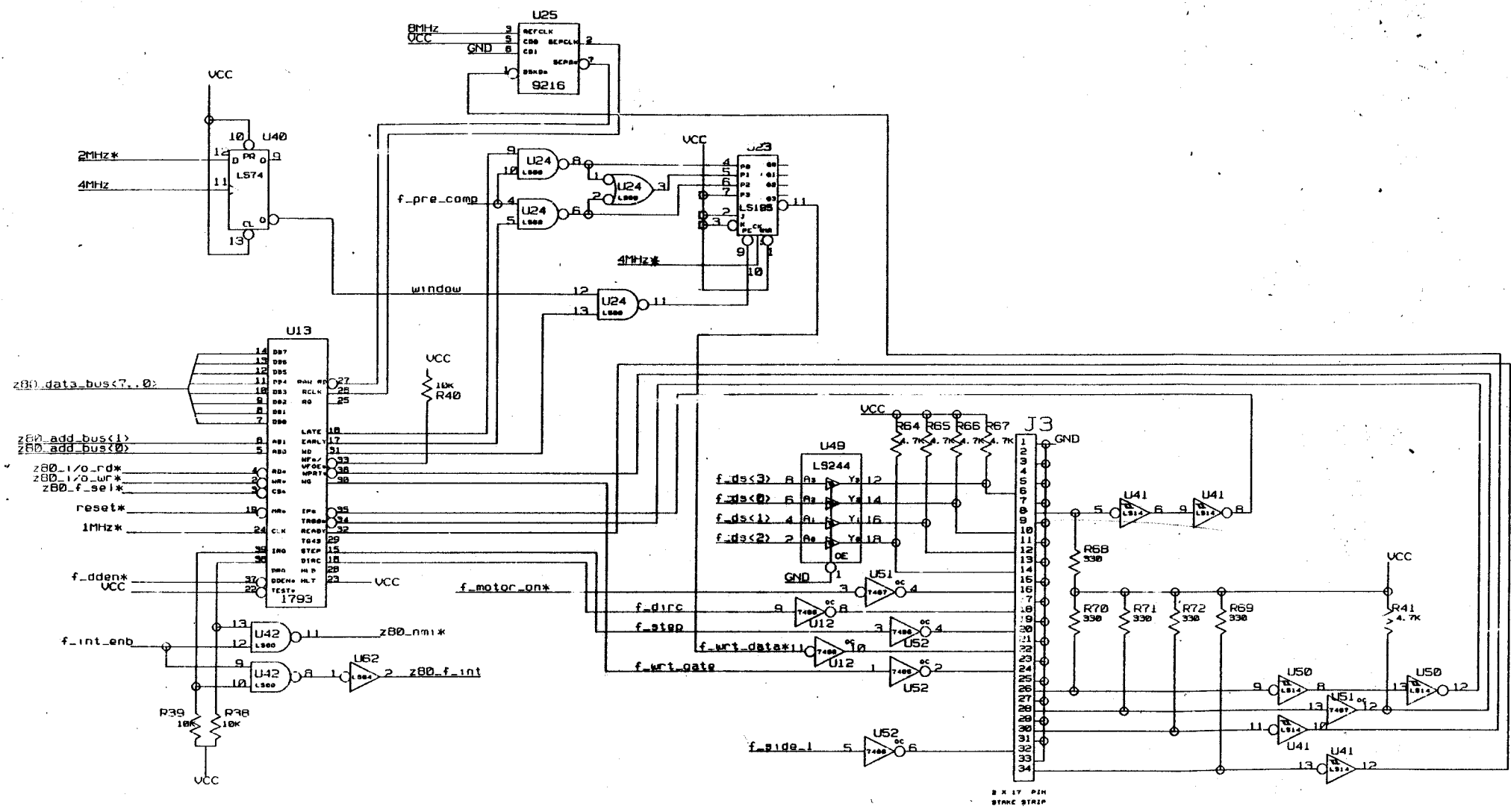
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PAGE: 1 of 13

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## SERIAL INTERFACE



## PARALLEL INTERFACE



FLOPPY DISC INTERFACE

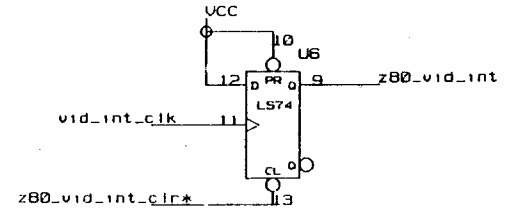
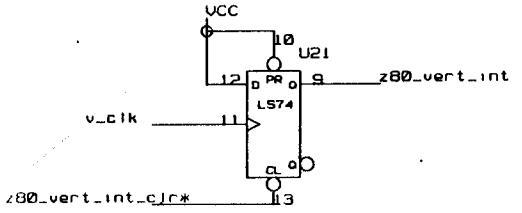
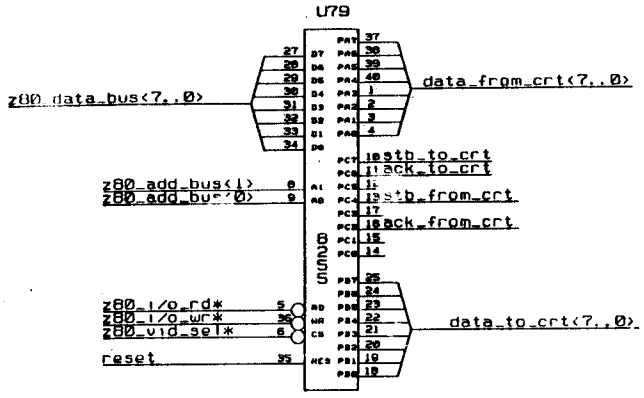
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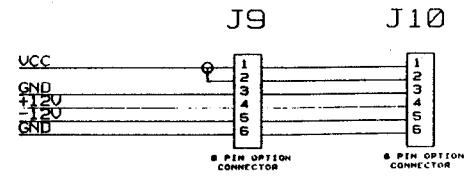
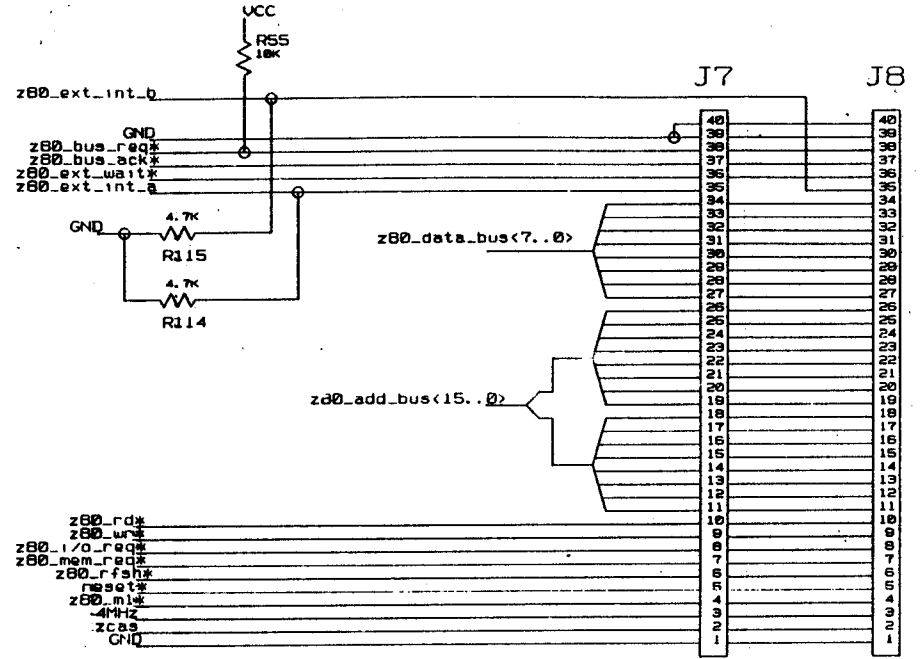
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INTERFACE TO CRT



OPTION CONNECTORS

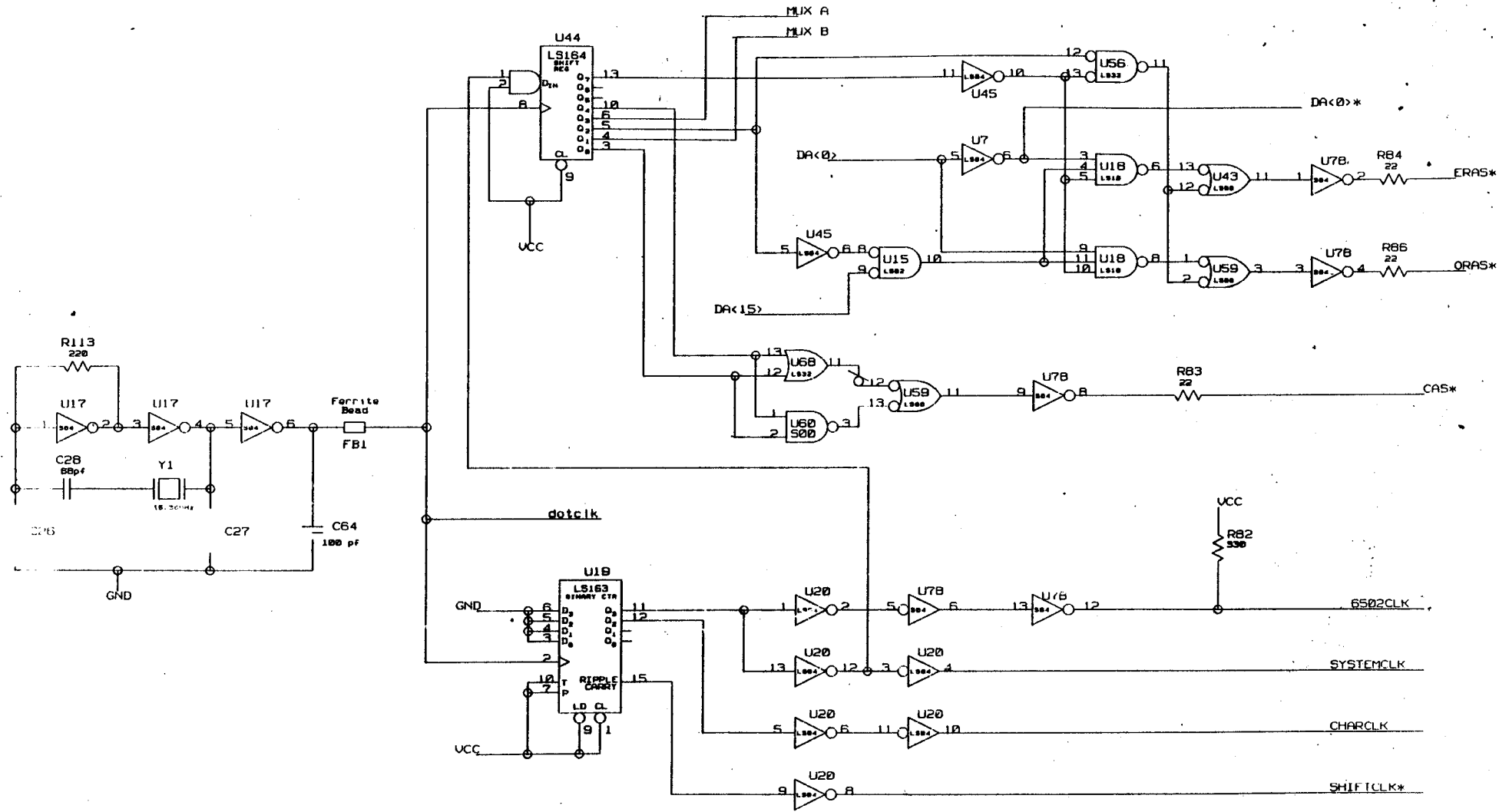
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VIDEO TIMING GENERATION

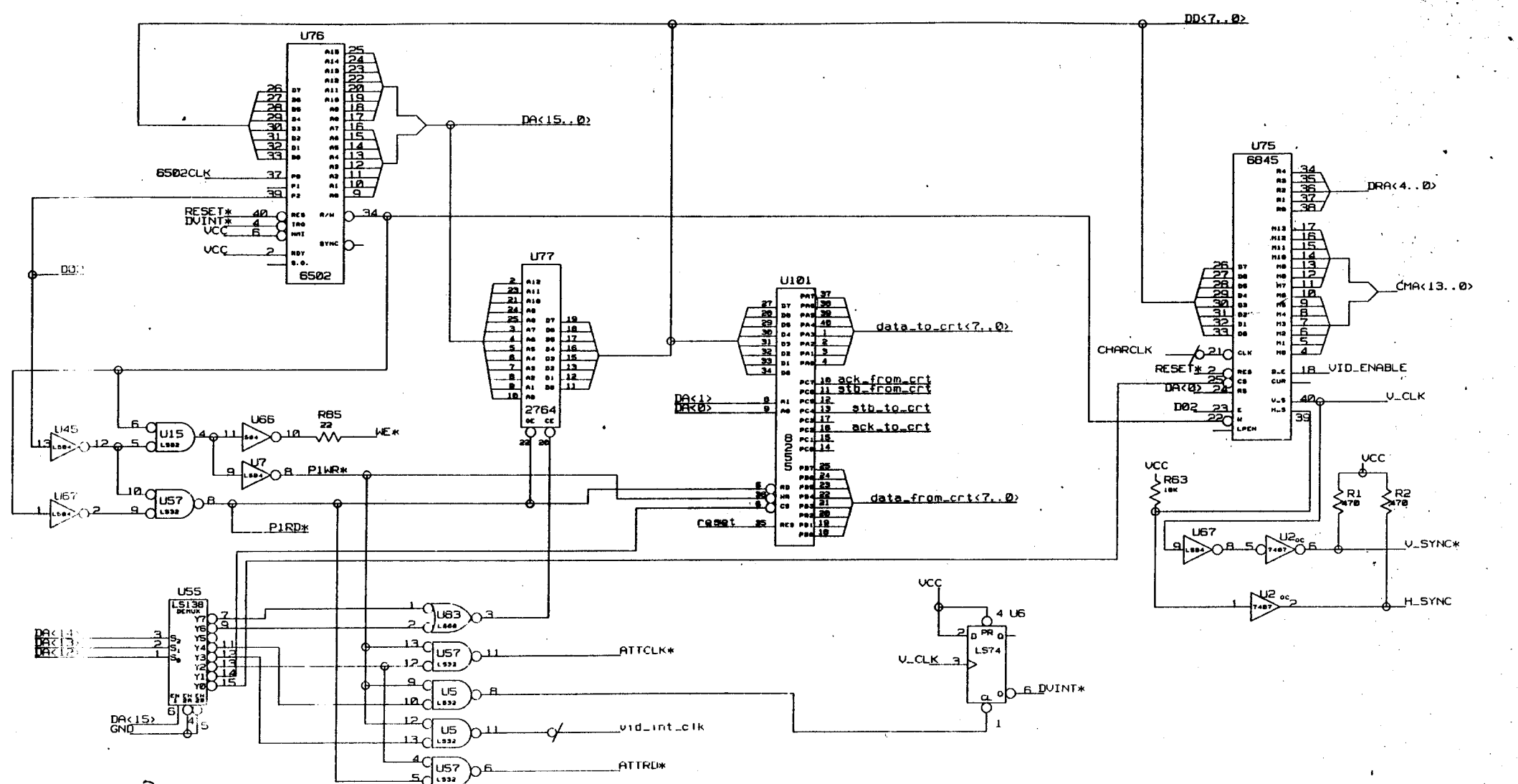
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6502 AND DISPLAY CONTROLLER

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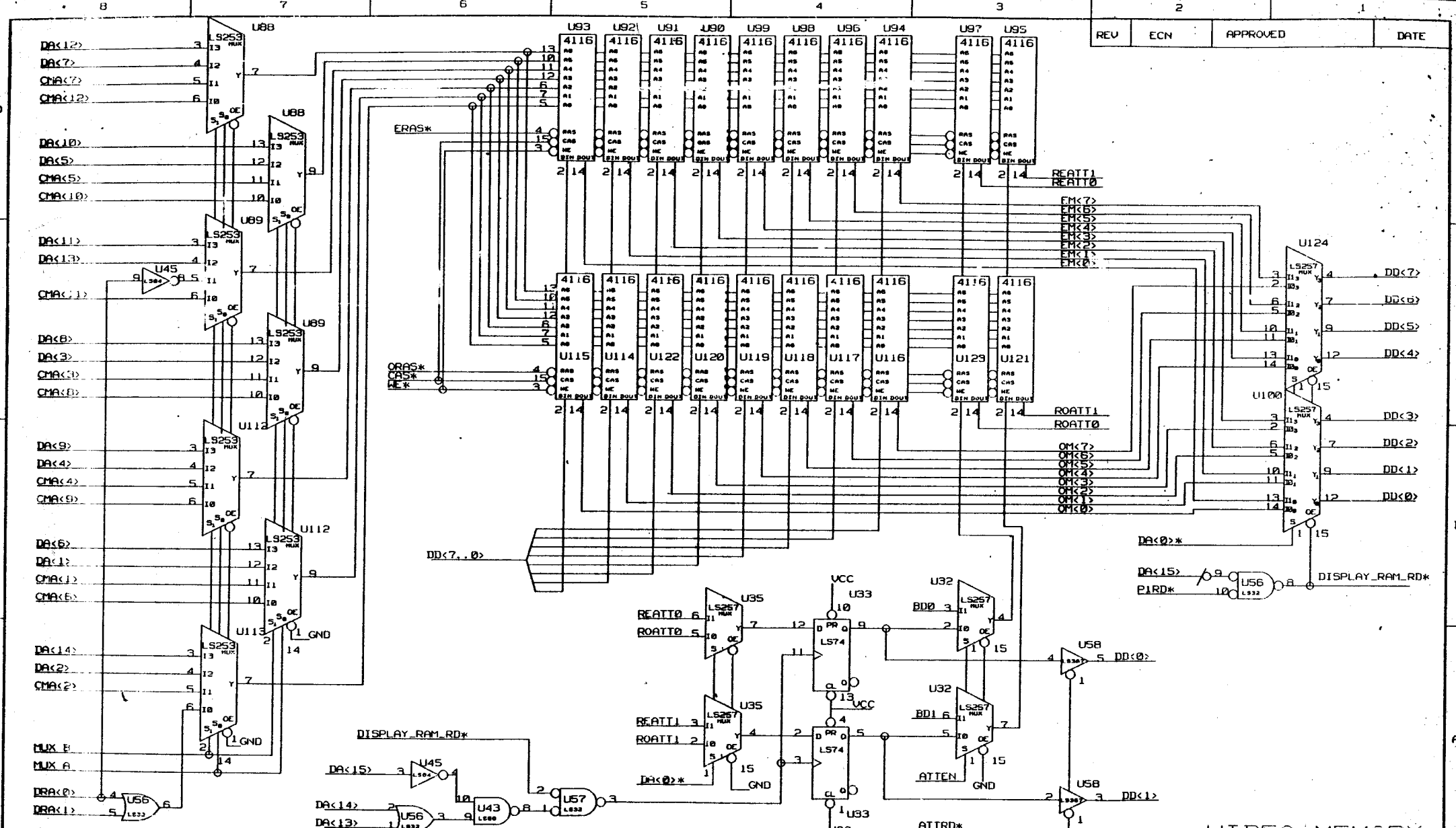
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VIDEO MEMORY

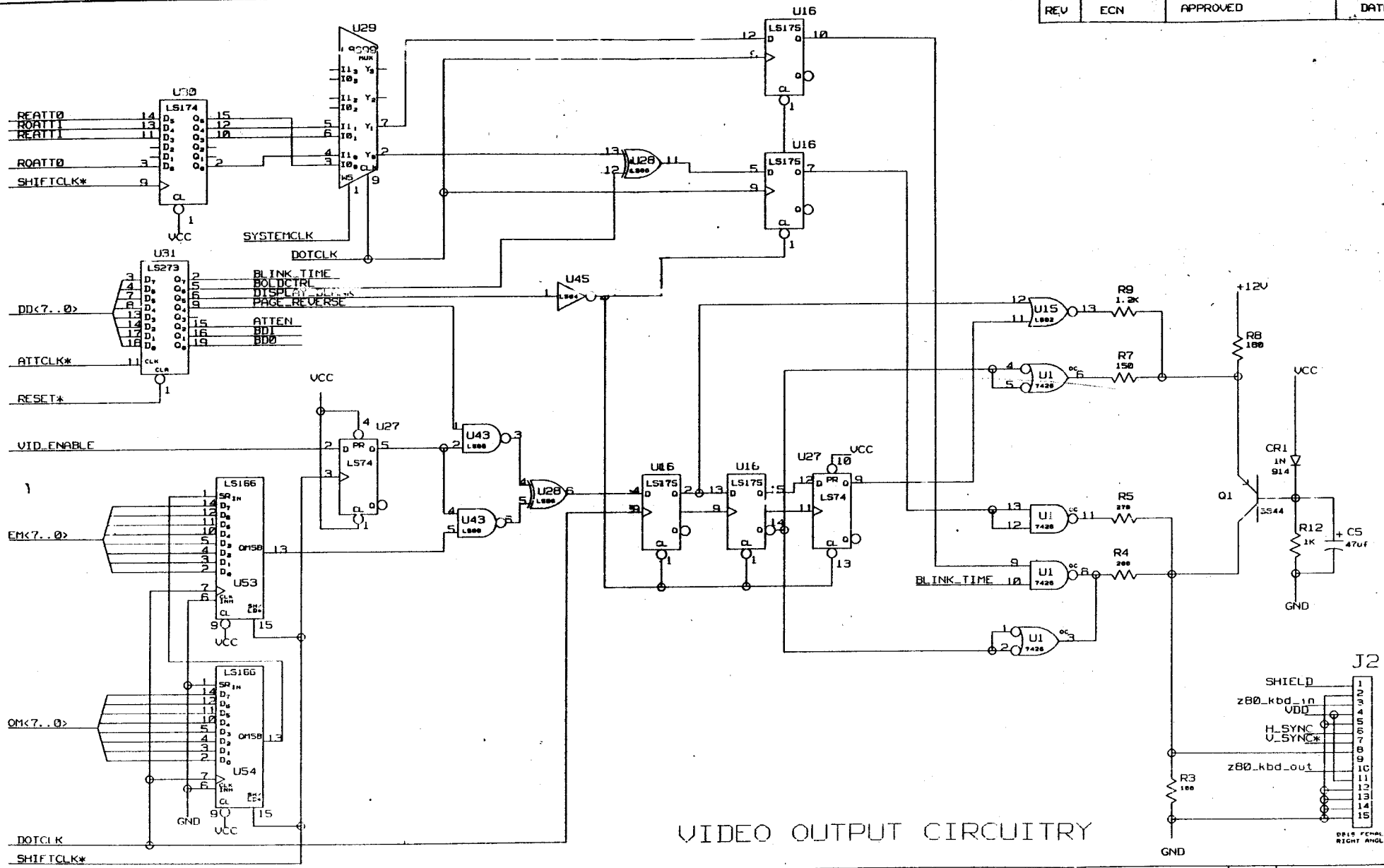
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VIDEO OUTPUT CIRCUITRY

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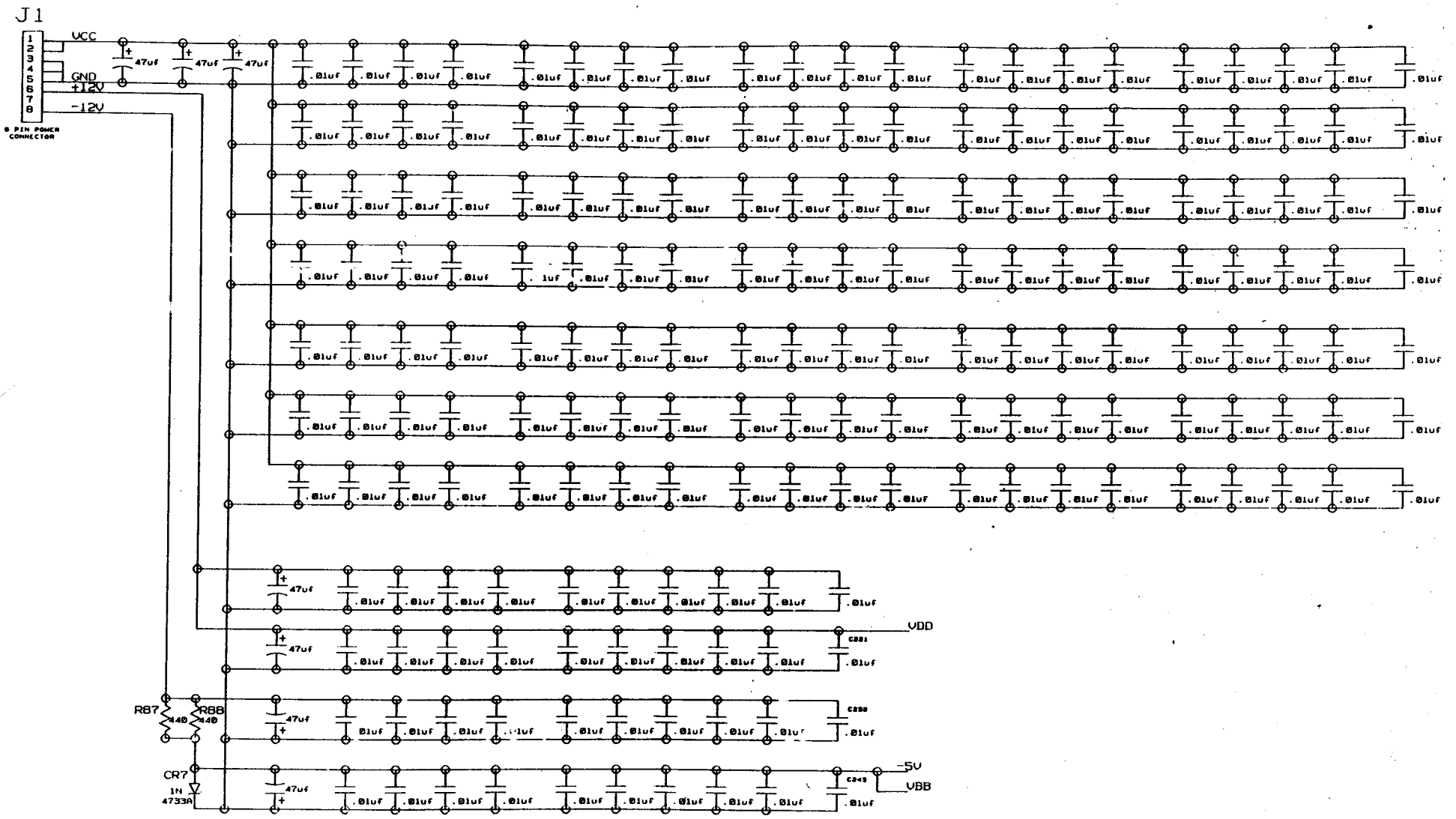
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# POWER CONNECTOR AND FILTER CAPS

REV	ECN	APPROVED	DATE
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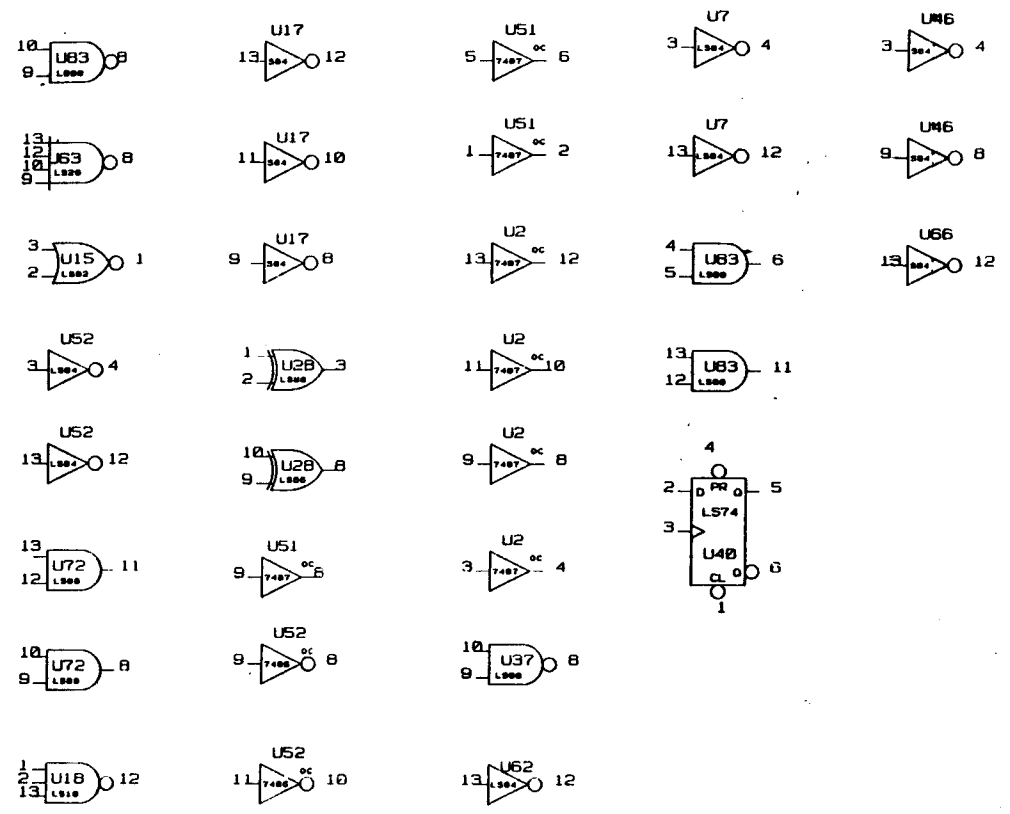
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SPARE GATES

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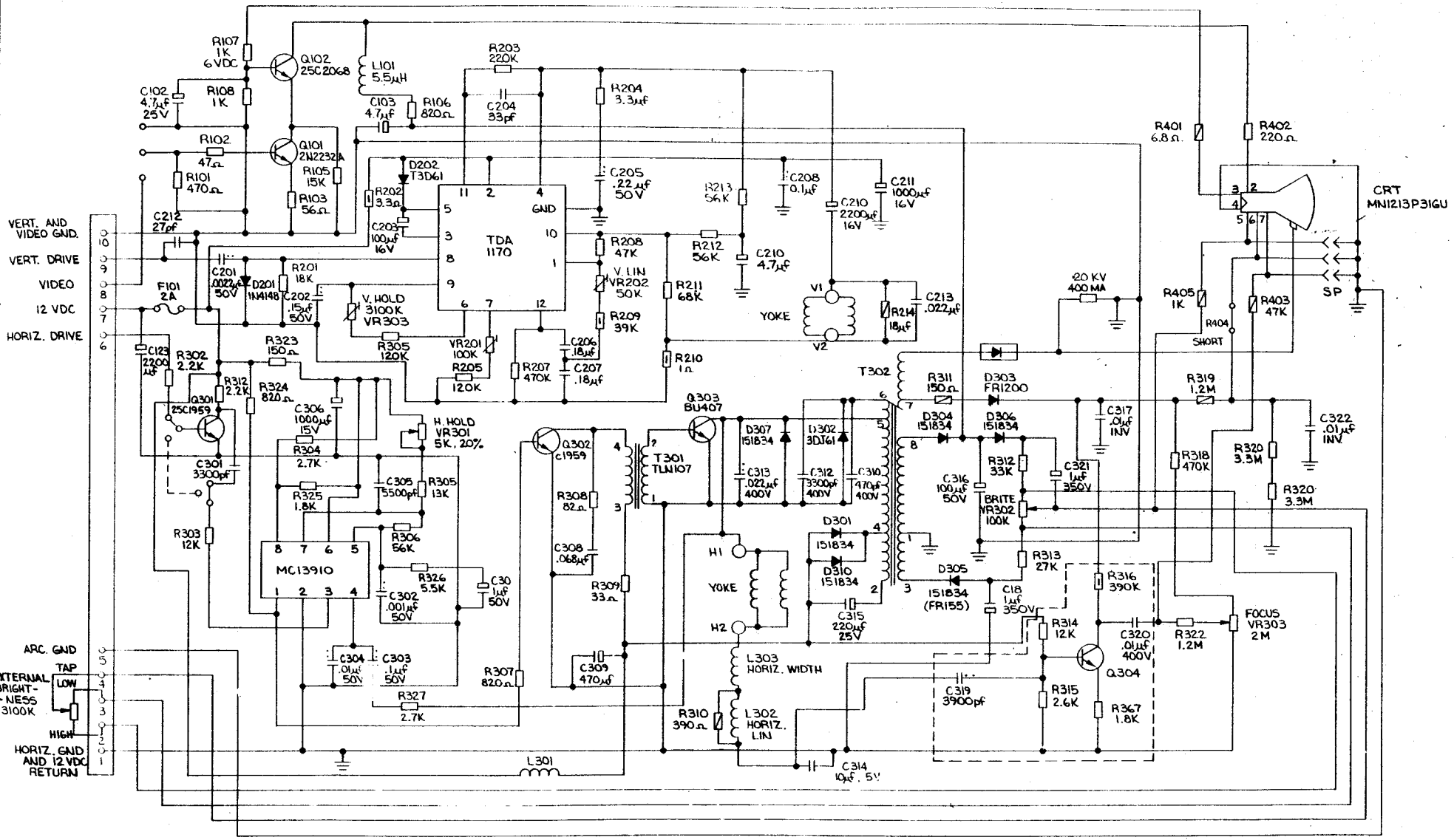
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REVISION STATUS			
REV	ZONE	DESCRIPTION	DATE APPR

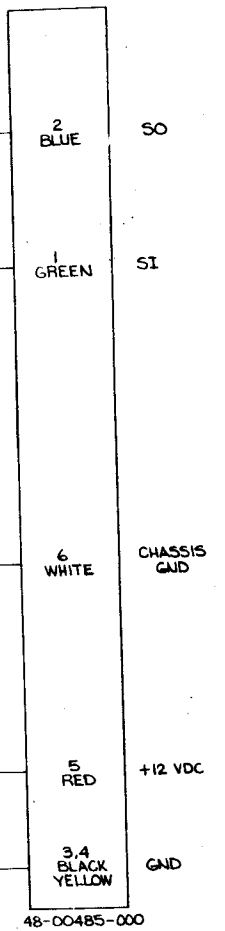
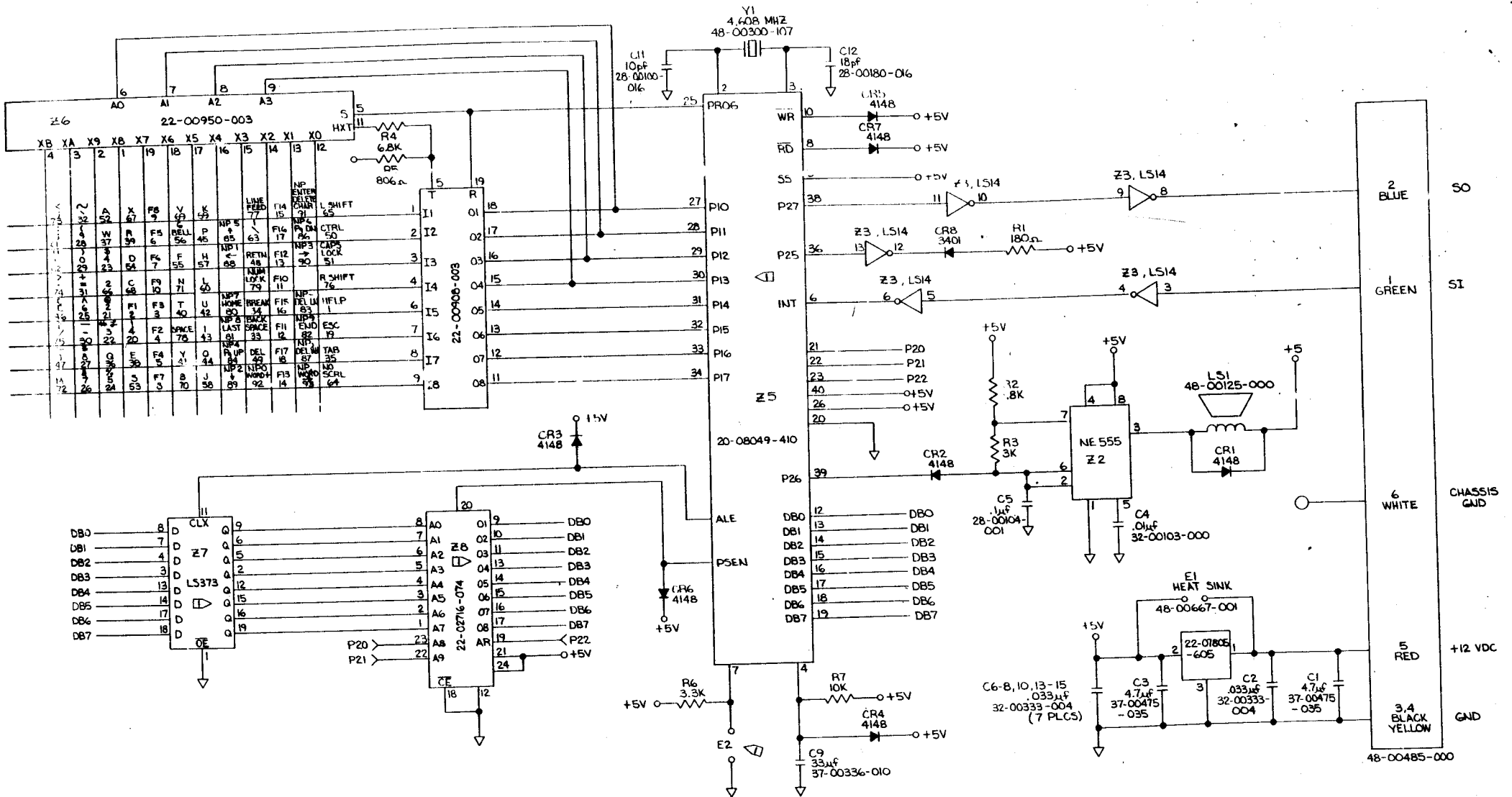


**SYMBOL DESCRIPTION**

- 1/4 W CARBON FILM RES.
- 1/2 W CARBON FILM RES. OR CARBON COMP. RES.
- 1 W METAL FILM RES. OR CARBON FILM RES.
- 2 W METAL OXIDE FILM RES.
- 3 W METAL OXIDE FILM RES.
- CERAMIC CAP.
- POLYESTER CAP.
- ELECTROLYTIC CAP.
- SPARK GAP
- VARIABLE RES.

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	<b>TITLE:</b> TATUNG MONITOR SCHEMATIC		<b>UNIT NO.</b> MN103-010	
	<b>Model No.</b> Next Assy.		<b>SCALE</b>  <b>SHEET</b>	
	<small>Visual Technology Incorporated          640 Main Street, Tisbury, MA. 01759</small>			

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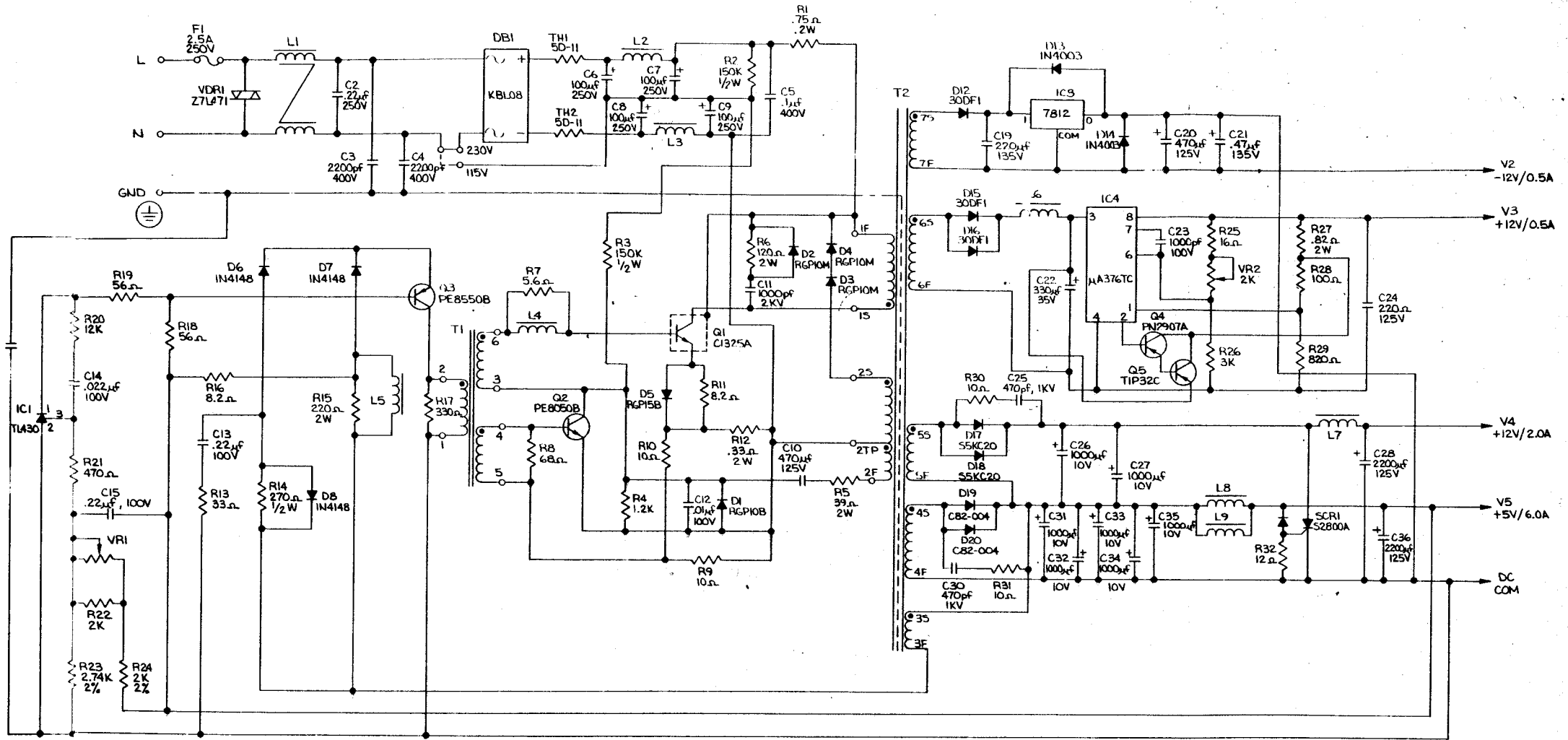


NOTES:

- ON -051 ASSY INSTALL 20-08039-000 AT Z5 AND INSTALL Z7 AND Z8. DELETE ETCH TIE AT E2.

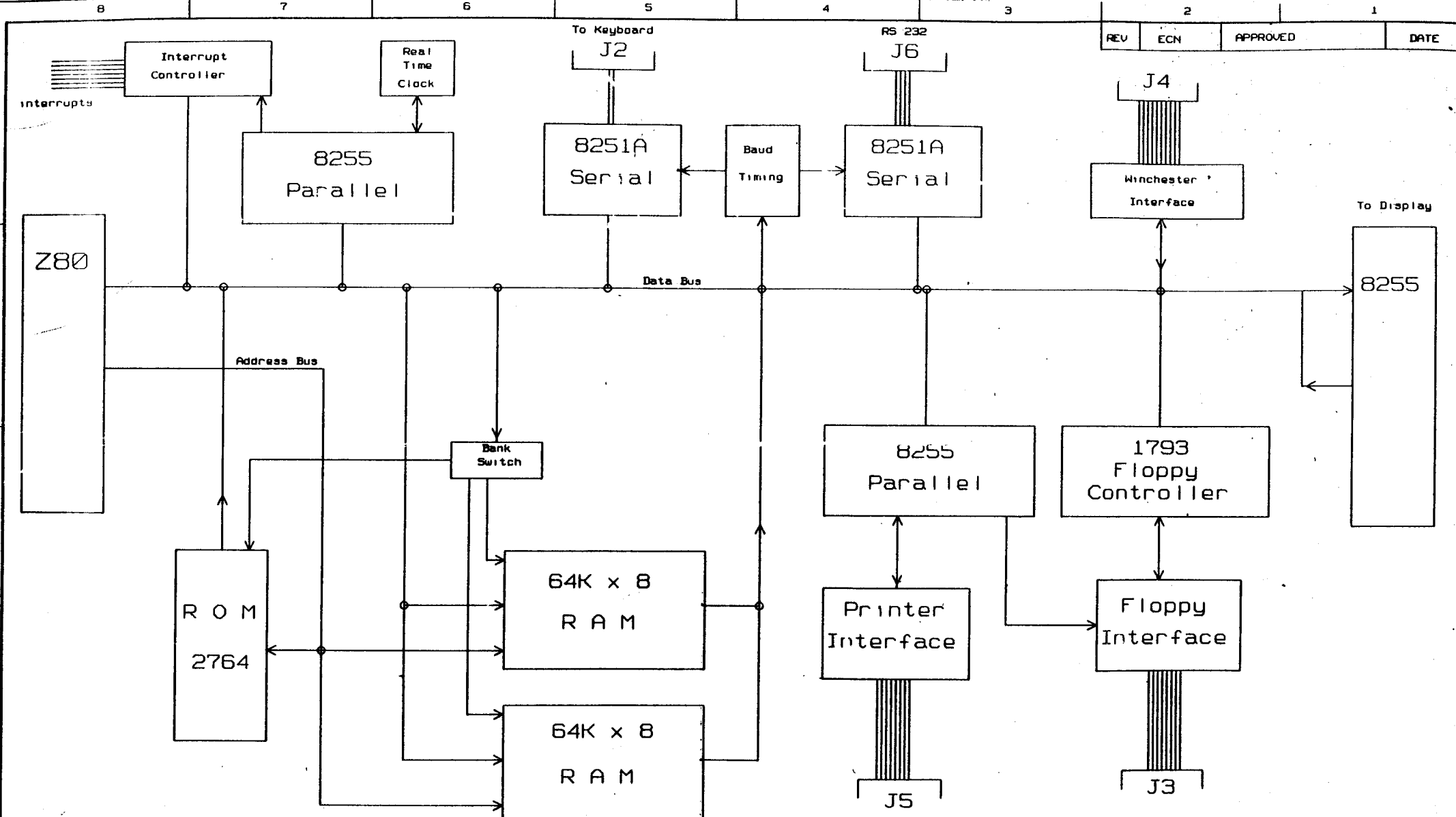
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NOTES:  
 1. ALL RESISTORS 1/4 W, UNLESS OTHERWISE NOTED.

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	CHECKED ENG Q.A. OPER	TITLE 75W POWER SUPPLY	UNIT NO. P5029-001	Model No. Next Assy.	SCALE 1:1



Z80 Processor Block Diagram

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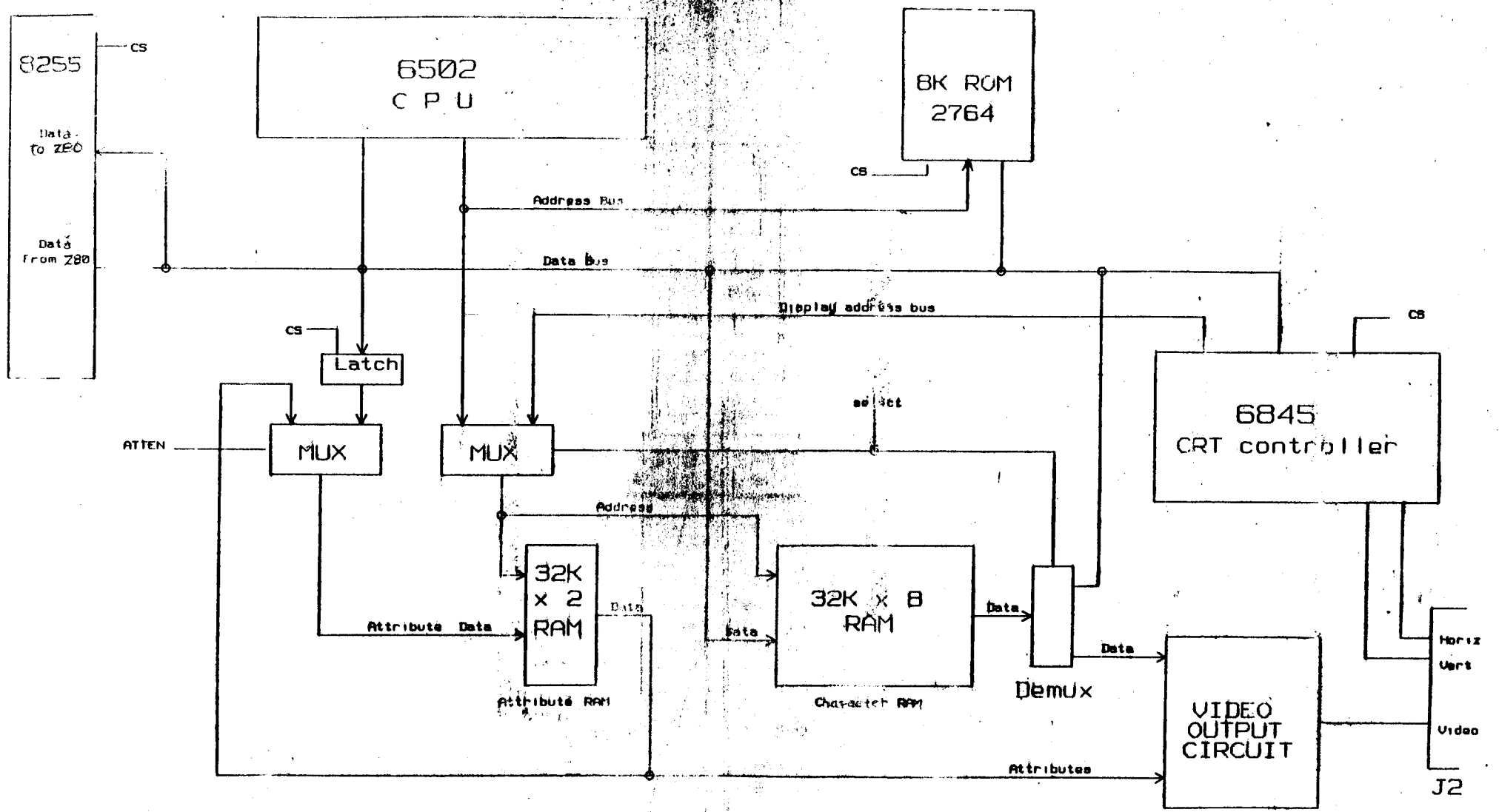
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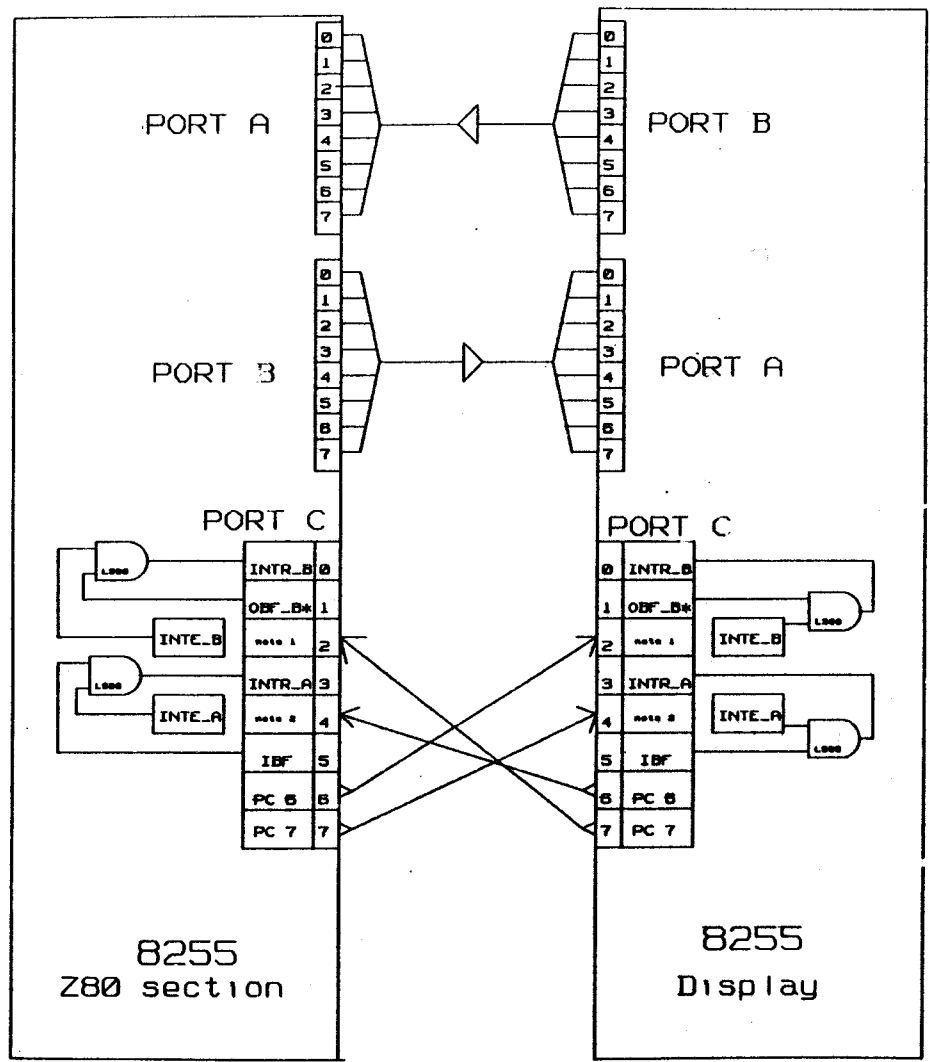
TITLE: V1050  
 Block Diagram

REV: 1A  
 DATE: 10/8/83  
 PAGE: 2 of





Display Block Diagram



note 1... This pin going low causes OBF\_B\* to go high

note 2... This pin going low latches data into port A and sets IBF high

6502 Initialization steps

- Initialize 8255 with mode byte B4H
- Set port C bit 2 high
- Set port C bit 4 high
- Set port C bit 6 high
- Set port C bit 7 high

Z80 Initialization steps

- Initialize 8255 with mode byte B4H
- Set port C bit 7 high
- Set port C bit 6 high
- Set port C bit 4 high
- Set port C bit 2 high

Send Data from Z80 section to Display section

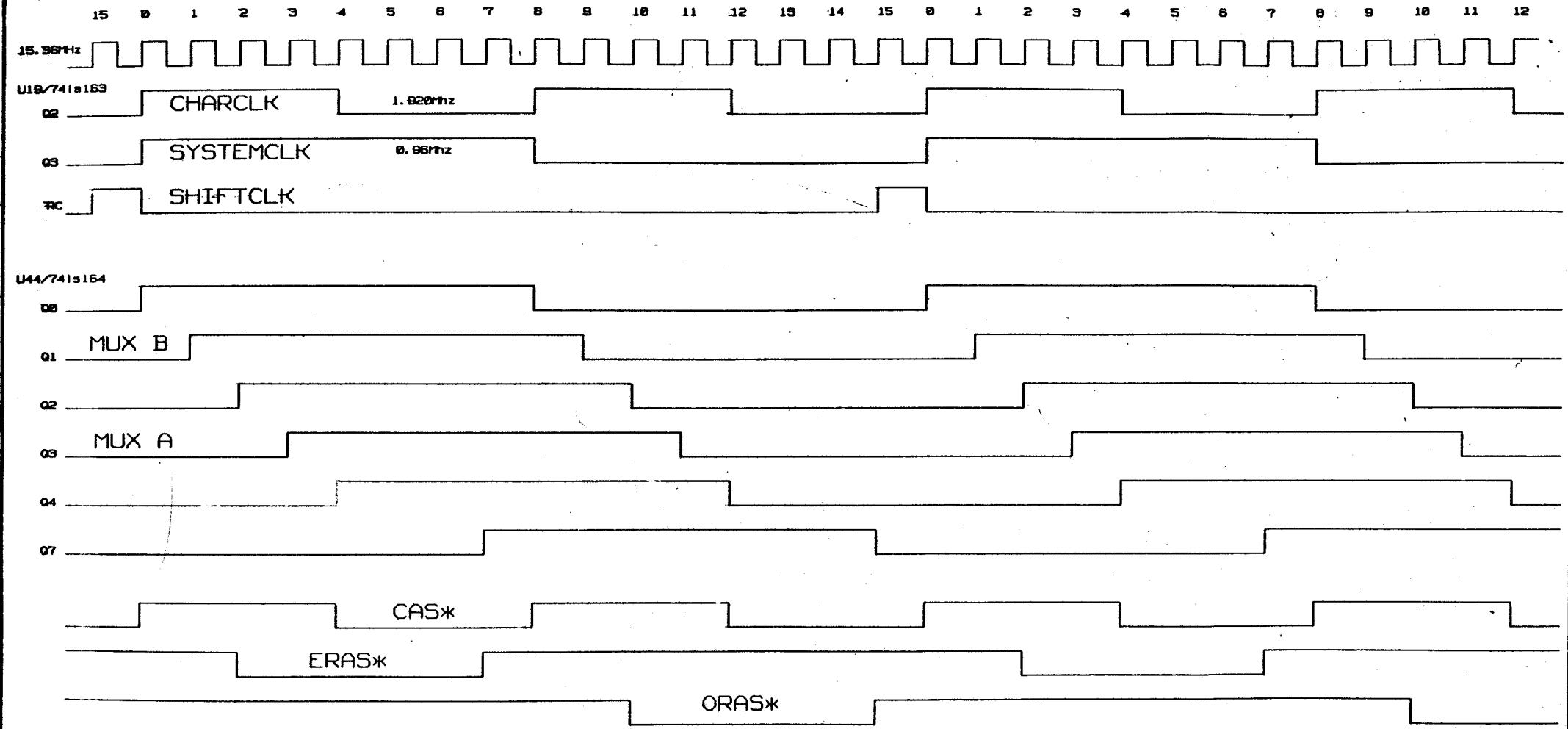
Z80 side of transfer:

1. Read port C
2. Check bit 0 (INTR\_B)
3. If equal to 0 then go back to step 2, if 1 continue  
Output character data to port B which sets Z80 OBF\_B\* low which in turn sets Z80 INTR\_B low
5. Set PC7 low which latches data into 6502 port A and sets 6502 IBF high
6. Set PC7 back to high which sets 6502 INTR\_A high

6502 side of transfer:

1. Read port C
2. Check bit 3 (INTR\_A)
3. If equal to 0 then go back to step 2, if 1 continue
4. Read port A (the character data) which clears 6502 IBF
5. Set PC7 to a 0 which sets Z80 OBF\_B\* high
6. Set PC7 back to 1

Z80 Processor to Display Interface



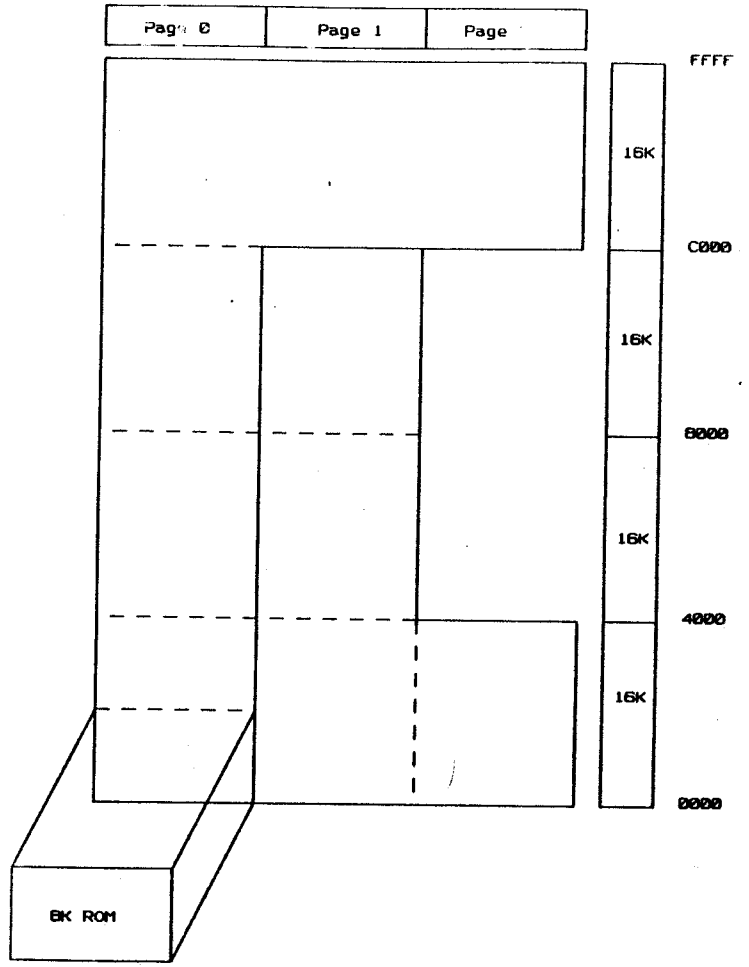
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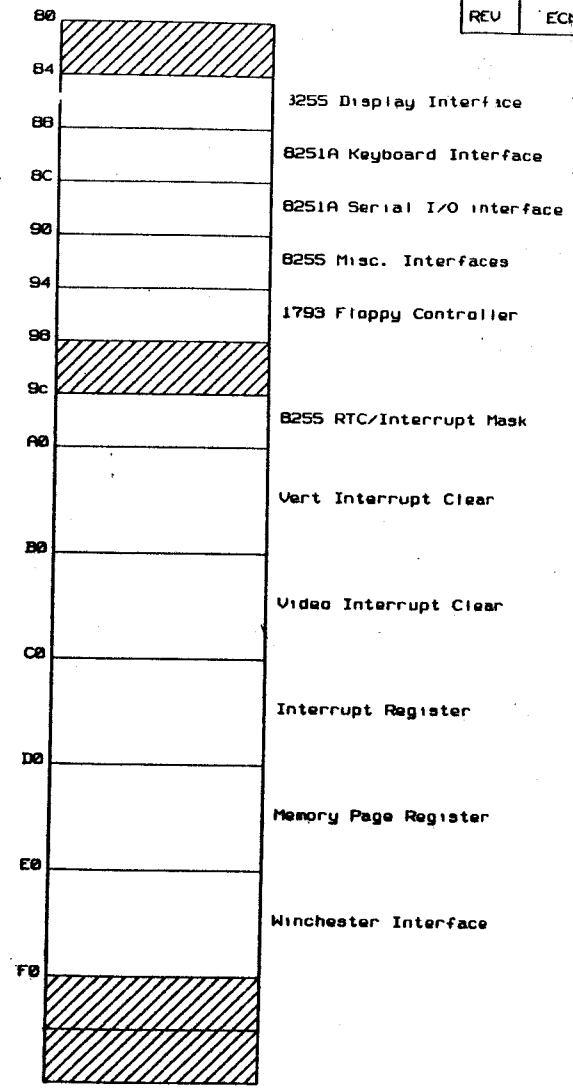
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V1050 Memory Map



V1050 I/O Map

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